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Enhancing Photoresponsivity of Self-Aligned MoS_2 Field-Effect Transistors by Piezo-Phototronic Effect from GaN Nanowires

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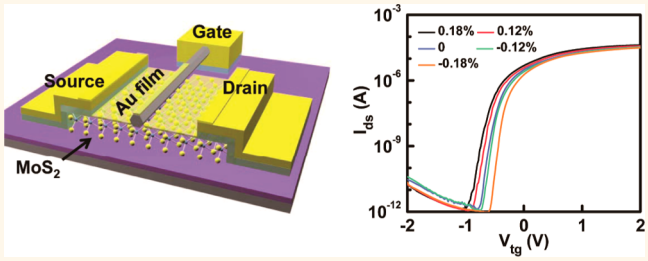
Supporting Information

ABSTRACT: We report high-performance self-aligned MoS_2 field-effect transistors (FETs) with enhanced photoresponsivity by the piezo-phototronic effect. The FETs are fabricated based on monolayer MoS_2 with a piezoelectric GaN nanowire (NW) as the local gate, and a self-aligned process is employed to define the source/drain electrodes. The fabrication method allows the preservation of the intrinsic property of MoS_2 and suppresses the scattering center density in the MoS_2/GaN interface, which results in high electrical and photoelectric performances. MoS_2 FETs with channel lengths of ~200 nm have been fabricated with a small subthreshold slope of 64 mV/dec. The photoresponsivity is 443.3 $A{\cdot}W^{-1}$, with a fast response and recovery time of ~5 ms under 550 nm light illumination. When strain is introduced into the GaN NW, the photoresponsivity is further enhanced to 734.5 $A{\cdot}W^{-1}$ and maintains consistent response and recovery time, which is comparable with that of the mechanical exfoliation of MoS_2 transistors. The approach presented here opens an avenue to high-performance top-gated piezo-enhanced MoS_2 photodetectors.



KEYWORDS: *piezo-phototronic effect, MoS_2, self-aligned, field-effect transistor, photodetector*

Monolayer MoS_2 possesses excellent electronic properties, good transparency, and robust mechanical flexibility[1−6] and is considered to be a promising candidate for electronic and optoelectronic applications.[7−13] MoS_2 field-effect transistors (FETs) with a high on−off ratio and photodetectors with high sensitivity have been demonstrated. However, the ambient absorption, interface trap density, and parasitic resistance and/or capacitance impact the performance of MoS_2 FETs, especially when the device size shrinks into the nanometer regime.[14] A self-aligned fabrication process has been proposed to be a precise and reliable device fabrication process to solve these problems.[15] Due to the band gap alignment of GaN nanowires (NWs) and MoS_2, GaN NWs form a p−n junction with chemical vapor deposition (CVD)-grown MoS_2. It functions as the local gate that can modulate the carrier transport in the MoS_2 channel. On the other hand, as a traditional piezoelectric material, the applied strain on GaN NWs can induce an internal piezoelectric potential,[16−18] which can not only serve as the gate potential to modulate the carrier transportation in the MoS_2 channel located underneath[19] but also impact the sensitivity of photodetectors that have been demonstrated to be a piezo-phototronic effect.[20,21]

Herein, we report high-performance self-aligned MoS_2 FETs with an on−off ratio of ~10^7 and a subthreshold slope (SS) as small as 64 mV/dec. The devices exhibit a photoresponsivity of 443.3 $A{\cdot}W^{-1}$ while maintaining a short response time of ~5 ms. Moreover, the photoresponsivity is further enhanced to 734.5 $A{\cdot}W^{-1}$ by the piezo-phototronic effect arising from the attached GaN NWs, and this value is comparable with that of mechanical exfoliation of MoS_2-based devices.[8] The strategy presented here is a rational coupling between MoS_2 and the piezo effect, and

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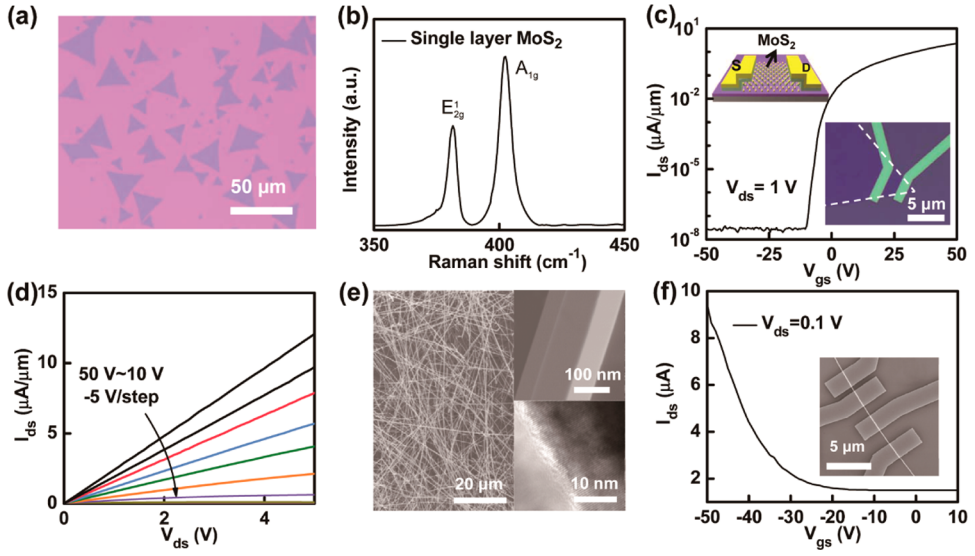

Figure 1. Characterization of a CVD-grown monolayer MoS_2 film and GaN NWs. (a) Individual monolayer MoS_2 triangles on the SiO_2/n^+-silicon substrate. (b) Raman spectra of CVD-grown monolayer MoS_2 shows a peak position difference of 20.5 cm^{-1} between two characteristic vibrating modes ($^1E_{2g}$ and A_{1g}). (c) Transfer curve of the MoS_2 FET with 300 nm SiO_2 as the dielectric layer. (d) Corresponding output characteristics of the MoS_2 FET. (e) SEM image of the as-prepared GaN NW. The insets present the orthohexagonal structure and the TEM image which indicates growth in the *c*-axis direction. (f) Typical transfer curve of a GaN NW transistor with the SEM image of the device in the inset.

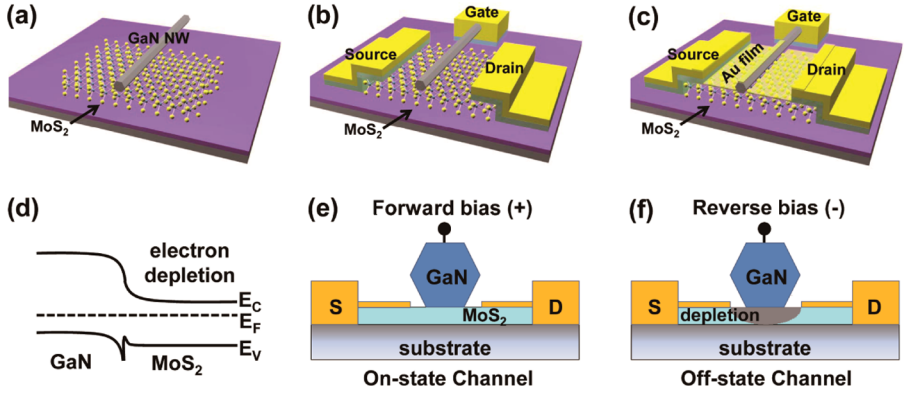

Figure 2. Schematic illustrations of the self-aligned fabrication process of the GaN NW top-gate MoS_2 FETs. (a) GaN NW is placed onto MoS_2. (b) Deposition of source, drain, and top-gate electrodes. (c) Deposition of 10 nm Au thin film on the MoS_2 channel *via* a self-aligned process. (d) Schematic energy band diagrams of a GaN NW on MoS_2. (e) Schematic illustrations of on-state channel at forward gate bias (charge conduction between S and D) and (f) off-state channel at reverse bias (depletion).

thus it opens a pathway to high-performance top-gated piezo-enhanced MoS_2 photodetectors without introducing appreciable defects.

RESULTS AND DISCUSSION

Monolayer MoS_2 films with sizes up to 50 μm are synthesized directly onto a SiO_2/n^+-Si substrate by the CVD approach, as shown in Figure 1a. Figure 1b shows the Raman spectra that confirm the monolayer characteristics of MoS_2 films, and the difference between the two $^1E_{2g}$ and A_{1g} modes is 20.5 cm^{-1}, suggesting that the synthesized films are monolayer. Back-gate MoS_2 FETs were fabricated, as shown in the insets of Figure 1c. The electrical performances were measured under dark conditions, and a typical transfer curve is shown in Figure 1c, indicating a large on−off ratio of ~10^8; the field-effect mobility is calculated to be 20.7 cm^2 V^{-1} s^{-1}. Figure 1d is the corresponding output curves, and the obvious pinch-off characteristics suggest that the MoS_2 active channel is fully modulated by the gate voltage. On the other hand, as a piezoelectric material, GaN NWs with good uniformity were synthesized *via* a CVD process and are ~100 μm long and 150−300 nm wide at the side, as shown in Figure 1e. The cross profile of the prepared GaN NWs is nearly orthohexagonal with a flat side surface (insets in Figure 1e) and present weak p-type transfer characteristics (Figure 1f), which enables compact contact between the GaN NW and MoS_2 for desirable gate coupling.

The physical assembly of self-aligned GaN NW gates can preserve the intrinsic property in MoS_2 and minimizes the access resistance. Figure 2a−c is the schematic images that illustrate the approach for fabricating self-aligned MoS_2-based piezo-FETs. Briefly, the as-prepared p-type GaN NWs were transferred onto MoS_2 film by a physical dry transfer process (Figure 2a).[15,22,23] Subsequently, the external source, drain, and gate electrodes were fabricated by e-beam lithography followed by metal deposition (Cr/Au, 10/70 nm), as shown in Figure

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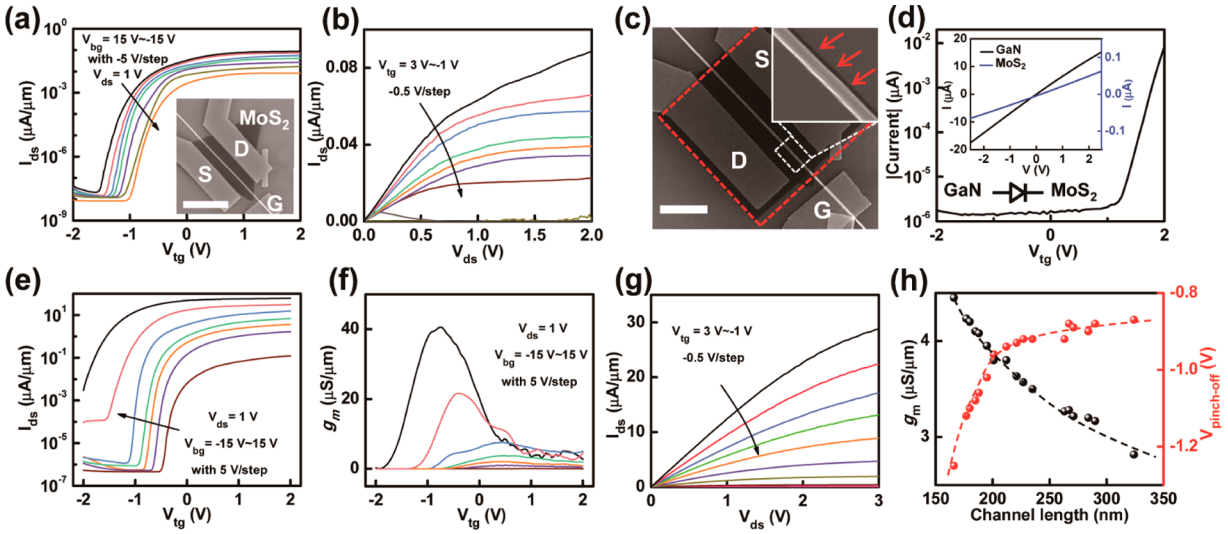

Figure 3. Electrical performance of the MoS_2 FETs. (a) Typical transfer characteristics of the MoS_2 FET with GaN NW as a local gate before depositing a 10 nm self-aligned Au film; the scale bar in the inset is 5 μm. (b) Typical output characteristics. (c) SEM image of the fabricated device; the scale bar is 2 μm. (d) Typical electrical performance of the GaN/MoS_2 device; the inset presents the electrical performance of GaN NW and MoS_2. (e,f) Transfer characteristics and transconductance *versus* V_{tg} bias at varying V_{bg}, respectively. (g) Typical output characteristics of the self-aligned MoS_2 FETs. (h) Transconductance and pinch-off voltage ($V_{pinch\text{-}off}$) as a function of channel length (L) for several devices.

2b. Finally, the self-aligned process was introduced by depositing a 10 nm Au film across the GaN NW onto the MoS_2 channel (Figure 2c). In the device configuration, the contact between MoS_2 and the GaN NW creates a p−n junction (Figure 2d), and the depletion layer at the MoS_2/GaN interface can prevent a significant gate leakage current. The GaN NW functioned as the self-aligned local gate of the MoS_2 piezo-FETs (Figure 2e,f).

Figure 3a shows the transfer characteristics of the devices without self-aligned electrodes under varied back-gate biases from −15 to +15 V, and the inset is the SEM image of the device. Positive back-gate biases move the pinch-off voltage ($V_{pinch\text{-}off}$) shift toward negative voltages, which is because the back-gate channel is formed, so a back-gate-induced channel current is superposed to the top-gate transfer curve. For negative back-gate biases, where the channel current is degraded, a much larger top-gate voltage is needed to compensate the original channel current than without a back-gate bias. Therefore, the top-gate pinch-off voltage shifts to more positive values. In other words, the positive back-gate voltage-induced electrostatic doping of MoS_2 reduces the contact resistance, leading to larger current. The dual-gate architecture may be an alternative solution to adjust the threshold voltage for integrated circuits[24] rather than local doping of an individual MoS_2 transistor.[25,26] Figure 3b is the output characteristics of the device, showing that the channel is efficiently modulated by the local GaN NW gate. However, since only a small amount of the MoS_2 channel is modulated by the local GaN NW gate and most of the channel is exposed in the atmosphere, the current is significantly impacted by the access resistance and impurity absorption, leading to an inferior dual-gate coupling effect. Figure 3c presents the SEM image of a self-aligned MoS_2 FET with a 200 nm GaN NW as the local gate. The device was then tilted 30°, and it is clearly shown that the GaN NWs can efficiently separate the Au metal into two parts (inset in Figure 3c). Therefore, the NW side width determines the L of the self-aligned MoS_2 FETs, so that the devices with much shorter L can be readily fabricated using NWs with smaller diameters. Electrical measurements on the MoS_2/GaN junction characteristics were carried out, and MoS_2 and GaN NWs show linear current−voltage characteristics (inset of Figure 3d), indicating no significant rectification characteristics and negligible contact resistance. The MoS_2/GaN junction shows clear rectification characteristics (Figure 3d), indicating an ideality factor of ~2.4.[27] Therefore, the MoS_2/GaN p−n junction can readily function as the local gate for MoS_2 piezo-FETs and prevent the gate leakage current from affecting the device performance (Supporting Information Figure S1).[28] Figure 3e shows top-gate sweep transfer curves of a typical device with self-aligned electrodes (L = 200 nm and W = 6 μm). The top-gate pinch-off voltage shifts from −0.5 to less than −2 V by applying a back-gate bias between −15 and +15 V, and the on−off ratio of all the curves is maintained at larger than 4 orders of magnitude. Notably, for V_{bg} = 0 V, SS is as small as 64 mV/dec at room temperature. The SS is given by

$$SS = \ln 10 \frac{kT}{q}(1 + (C_s + qD_{it})/C_{ox})$$

where C_s is the capacitance of MoS_2, D_{it} is the interface trap density, and C_{ox} is the gate capacitance. As C_s is negligible in the deep-subthreshold region, qD_{it}/C_{ox} is only about 0.07, partially indicating low densities of charges and a scattering center in the interface, while the device operation mechanism also allows scattering-minimized transport without gate-charging-induced interferences.[29] The transconductance is correspondingly affected by the applied back-gate voltage, which is induced by electrostatic capacitive coupling and the formation of a secondary channel, as shown in Figure 3f. The self-aligned MoS_2 FETs show obvious saturation behavior, which may come from the built-in electric-field-induced depletion layer of the MoS_2/GaN NW p−n junction (Figure 3g). At low V_{ds}, the linear behavior suggests ohmic contact between MoS_2 and the source/drain electrodes. During the measurement, the back-gate is ground to avoid the capacitance coupling effect. At V_{ds} = 3 V, the drain current is 28.3 μA/μm at 3 V top-gate voltage,

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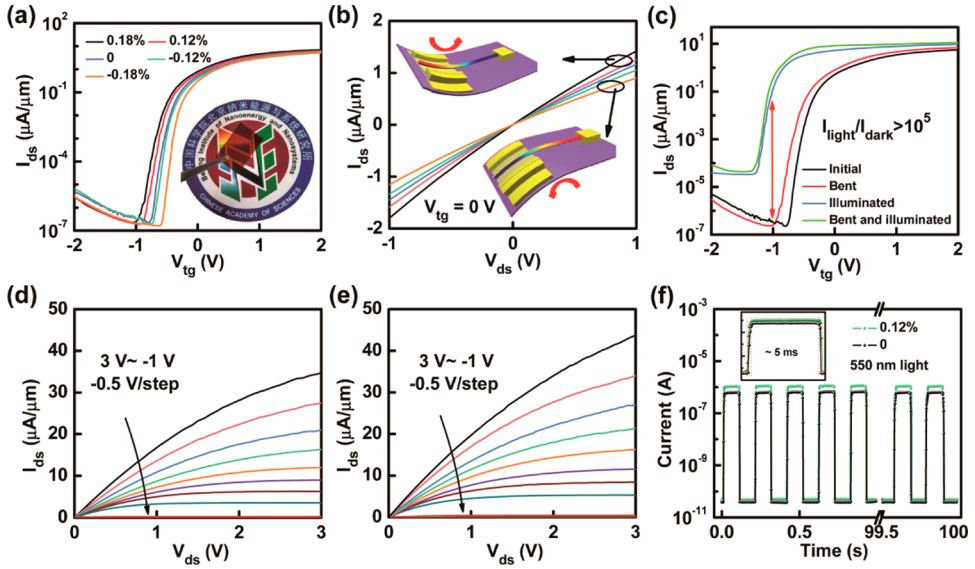

Figure 4. Electrical and photoelectric performance of the self-aligned MoS_2 FETs on Kapton. (a) Transfer characteristics of the self-aligned MoS_2 FETs under strain; the inset is the optical image of the devices on the flexible Kapton substrate (institute logo used with permission). (b) Output curves of the self-aligned MoS_2 FETs without external gate voltage under different applied strain. Insets depict the effect of strain on the GaN NW gate. Gradient ramp indicates the piezo-potential in GaN NW; red and blue indicate positive and negative piezo-potential, respectively. (c) Transfer curves of the same self-aligned MoS_2 FETs under different test conditions. (d,e) Output characteristics of the self-aligned MoS_2 FETs under 550 nm light illumination and bending with light illumination, respectively. (f) On−off photoresponse of the self-aligned MoS_2 FETs with (cyan curve) and without (black curve) external applied strain.

and the output current is more than 100 times larger than that in the previous self-aligned metal deposition. This confirms that depositing metal thin film onto the MoS_2 channel can effectively reduce the access resistance. Notably, such a high current density is comparable with that of the devices using high-k materials as a dielectric layer.[1,4,7,30,31] Figure 3h shows a summary of transconductance and pinch-off voltage of self-aligned MoS_2 piezo-FETs as a function of L ranging from 166 to 324 nm. The transconductance approaching 4.5 $\mu S/\mu m$ is obtained for the 166 nm channel length device. The pinch-off voltage stays around −1 V as the variation of channel length, indicating a reliable and reproducible device fabrication strategy. Nevertheless, improved electrical performance still can be further promoted by reducing the resistance of GaN NWs.

As aforementioned, the small SS indicates that GaN NWs can form a low trap density interface with MoS_2, which can function as the local gate of the self-aligned MoS_2 piezo-FETs. Furthermore, due to the non-centrosymmetric structure of GaN, the piezo-potential inside the volume can be induced by introducing deformation on the NW. After a quantitative analysis of electrical characteristics of the MoS_2 piezo-FETs without introducing strain on the rigid substrate, we investigated the piezo-potential of a GaN NW on the electrical and photoelectric performances of the MoS_2 piezo-FETs.[32] To realize efficient piezo effect coupling, the GaN NWs were unevenly transferred onto MoS_2 to fabricate MoS_2 piezo-FETs.[21,33] It is important to note that the Au deposited on the top surface of the GaN nanowire may screen the local piezo-potential at the top, but the potential next to the MoS_2 can effectively be used for the gating effect. Figure 4a shows the transfer characteristics of a 210 nm channel length device, and the on-current density is comparable with that of the similar device on a SiO_2/Si substrate. Insets in Figure 4b depict the method for introducing a deformation in a GaN NW gate. The transfer curves changed under different applied strain because of the polarization-induced internal field created by the applied strain on the piezoelectric GaN NW local gate. Figure 4b shows the output characteristics of the device with different applied strain under zero external gate voltage. As the GaN NW effectively generates a negative potential when it was tensile stressed, the piezo-FET has a decreased I_{ds} when compared to the piezo-FET without strain. In contrast, compressive strain will enhance I_{ds} to introduce a positive potential. Moreover, even if the serial deformations increased from 0 to 0.18%, the I_{ds} presents consistent changes. In addition, the values of strain in the GaN NWs were evaluated by employing the Saint-Venant bending theory for small deflections.[21]

Strain-induced inner-crystal piezo-potential can be employed to modulate the carrier transportation and photodetector performance, which is known as the piezo-phototronic effect.[19,21,34] As a demonstration of the concept, 550 nm light with a power density of 1.2 mW/mm^2 was illuminated on the device under 0.18% compressive strain, and Figure 4c displays the photoinduced transfer curves of the self-aligned MoS_2 piezo-FETs (blue line), indicating a clear enhancement of on-current with the pinch-off voltage shifted to about −1.3 V. Moreover, the hysteresis is as small as 0.15 V, and the $\Delta V_{pinch\text{-}off}$ of the hysteresis transfer curves was slightly changed under various measurement conditions (Supporting Information Figure S2). The output performance of the self-aligned MoS_2 piezo-FETs under various measurement conditions is shown in Figure 4d,e, which indicates the output characteristics with light illumination and with light illumination under 0.18% compressive strain. The obvious enhancement of output current indicates that the piezo effect can significantly impact the output current of the device under light illumination. Such a pinch-off voltage shift and on-current enhancement by the piezo effect enable the implementation of high signal-to-noise ratio photodetectors.[20,35] To maximize the photocurrent gain,

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the top-gate was first biased by applying −1 V to pinch-off the channel, so that the devices obtained a large photoresponse ratio (I_{light}/I_{dark}).[36,37] According to dynamic photoswitching behavior with 5 Hz light switching in Figure 4f, the fast response time of ∼5 ms is obtained. Moreover, the respective photoresponse ratio is estimated to be $\sim 10^5$ (black curve). Table 1 summarizes the performance of the previously reported

Table 1. Summary of Dynamic Switching Performances Measured from MoS_2-Based Phototransistors at Room Temperature

ref	I_{light}/I_{dark}	response time	wavelength	photoresponsivity
this work	$\sim 10^5$	5 ms	550 nm	734.5 A·W^{-1}
3	unknown	50 ms	550 nm	7.5×10^{-3} A·W^{-1}
7	$<10^2$	1.5 s	580 nm	unknown
8	unknown	9 s	561 nm	880 A·W^{-1}
38	$\sim 10^3$	2 ms	635 nm	2570 A·W^{-1}
39	10^5	60 s	DUV light	0.4 A·W^{-1}
40	$\sim 10^5$	0.3 s	405 nm	1.98 A·W^{-1}
41	$\sim 10^3$	unknown	633 nm	1.42 A·W^{-1}
42	unknown	0.28 s	632.8 nm	∼10 A·W^{-1}
43	<10	unknown	450 nm	2.3 A·W^{-1}
44	$\sim 10^2$	unknown	638 nm	342.6 A·W^{-1}
45	$\sim 10^3$	unknown	633 nm	0.12 A·W^{-1}
46	2.85×10^3	2 ms	520 nm	1.1 A·W^{-1}

MoS_2-based photodetectors, which ensures the superior performance of the self-aligned MoS_2 piezo-FETs.[3,7,8,38−45] Additionally, the built-in electric field in the MoS_2/GaN NW p−n junction can efficiently pinch-off the channel at zero gate voltage, so that the MoS_2 piezo-FETs can eliminate the persistent asymmetric photocurrent, resulting in fast recovery time.[8,45,46] Here, the photoresponsivity is estimated to be about 443.3 A·W^{-1}. Specifically, the majority of the MoS_2 channel is covered by the opaque GaN NW; the calculated incident power is larger than the actual value, so the actual photoresponsivity should be much larger than this value. Moreover, with a deformation of 0.18%, the piezo-phototronic-induced photocurrent enhancement effect results in an improved photocurrent of 1.11 μA under the same illumination conditions, as shown in Figure 4f (cyan curve). Therefore, according to the time domain plot, the photoresponsivity should be enhanced to 734.5 A·W^{-1}.

CONCLUSION

In summary, self-aligned MoS_2 piezo-FETs with channel lengths around 200 nm have been fabricated by using GaN NWs as the local gate with a physical self-aligned method, in which the MoS_2 and GaN NWs were prepared *via* a CVD approach. The devices obtained high electrical performance and low interface trap density, which is comparable to that of mechanical exfoliation of MoS_2 devices. The piezo-FETs exhibit fast photoswitching in 5 ms as photodetectors, and the photoresponsivity was further enhanced by the piezo-phototronic effect from GaN NWs. We conclude that the piezoelectric potential-gated MoS_2 piezo-FETs would be a promising model nanotransistor with high performance for nanoelectronics and nano-optoelectronics.

METHODS

Growth of Monolayer MoS_2 and GaN NWs. The MoO_3 powder was placed into a quartz boat and put into the reacting furnace as the downstream source. A 300 nm SiO_2-coated n^+-silicon substrate was placed on top of it as the growth substrate, and the sulfur powder was placed upstream of argon. The furnace was first purged with 50 sccm of argon for 10 min, and the pressure of the tube was maintained at 1 kPa with argon flow of 50 sccm throughout the whole process. Then the temperature of the MoO_3 powder was set to 850 °C at a rate of 30 °C/min. Subsequently, the temperature of sulfur powder was set to 150 °C and kept for 5 min. Finally, the furnace was naturally cooled under the protection of argon atmosphere. The CVD method was used for fabricating the GaN NWs and was carried out in a tubular furnace with a controlled atmosphere. Typically, Ga_2O_3 powder with a purity of 99.99% and NH_3 (99.999%) gas were utilized as the Ga and N sources. First, the Ga_2O_3 powder was placed in an alumina boat and pushed into the tubular furnace. Five nanometer Au was deposited onto the sapphire by an e-beam evaporator, and the substrate was put downstream. The reactor was pumped to 5 Pa and flushed with nitrogen gas to eliminate the residual oxygen. Then, the pressure of the system was kept constant at 1 bar before being heated to 1100 °C, and 50 sccm N_2 flow was introduced to the furnace. At 1100 °C, the N_2 was replaced by 250 sccm NH_3 and maintained for 180 min. Finally, the presence of N_2 was resumed in the furnace with a flow rate of 50 sccm. Finally, the furnace was naturally cooled under the protection of a N_2 atmosphere.

Device Fabrication. For flexible device fabrication, poly(methyl methacrylate) (PMMA) film was covered onto the prepared MoS_2 with a spin-coating method at 4000 rpm and then baked at 150 °C for 5 min. Subsequently, the cut piece was immersed into 1 M KOH solution for several hours to etch the SiO_2/Si substrate. After that, the released PMMA membrane floated on the solution and could be transferred onto the Kapton substrate. Next, PMMA was dissolved in acetone. Finally, the self-aligned MoS_2 FETs were fabricated with the same method as that on the rigid substrate.

Characterizations. The wavelength of the excitation laser used in Raman characteristics was 532 nm. All electrical measurements were carried out by combining a Keithley 4200-SCS probe station under atmospheric conditions. The deformation of the devices was controlled by moving the holder onto a 3D displacement table. During the optical measurements, the whole substrate was globally illuminated by the incident laser.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.6b01839.

Gate leakage current of the self-aligned MoS_2 FET; comparison of the transfer characteristics of the same device under different test conditions (PDF)

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Author Contributions

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Notes

The authors declare no competing financial interest.

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