In$_2$O$_3$ Nanowire Field-Effect Transistors with Sub-60 mV/dec Subthreshold Swing Stemming from Negative Capacitance and Their Logic Applications

Qian Xu, Xingqiang Liu, Bensong Wan, Zheng Yang, Fangtao Li, Junfeng Lu, Guofeng Hu, Caofeng Pan, and Zhong Lin Wang

†CAS Center for Excellence in Nanoscience, Beijing Key Laboratory of Micro-nano Energy and Sensor, Beijing Institute of Nanoenergy and Nanosystems, Chinese Academy of Sciences, Beijing 100083, P. R. China
‡School of Nanoscience and Technology, University of Chinese Academy of Sciences, Beijing 100049, P. R. China
§School of Physics and Electronics, Hunan University, Changsha 410082, P. R. China
∥Center on Nanoenergy Research, School of Physical Science and Technology, Guangxi University, Nanning, Guangxi 530004, P. R. China
⊥School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta, Georgia 30332, United States

ABSTRACT: Heat dissipation is a key issue for scaling metal-oxide-semiconductor field-effect transistors (MOSFETs). The Boltzmann distribution of electrons imposes a physical limit on the subthreshold swing (SS), which impedes both the reduction of the switching energy and the further increase of the device density. The negative capacitance effect is proposed to rescue MOSFETs from this phenomenon called “Boltzmann tyranny”. Herein, we report In$_2$O$_3$ nanowire (NW) transistors with SS values in the sub-60 mV/dec region, which utilize the ferroelectric P(VDF-TrFE) as the dielectric layer. An ultralow SS down to $\sim 10$ mV/dec is observed and spans over 5 orders of magnitude in the drain current. Meanwhile, a high on/off ratio of more than $10^8$ and a transconductance ($g_m$) of 2.3 $\mu$S are obtained simultaneously at $V_d = 0.1$ V. The results can be understood by the “voltage amplification” effect induced from the negative capacitance effect. Moreover, the steep slope FET-based inverters indicate a high voltage gain of 41.6. In addition to the NOR and NAND gates, the Schmitt trigger inverters containing only one steep slope FET are demonstrated. This work demonstrates an avenue for low-power circuit design with a steep SS.

KEYWORDS: field-effect transistors, subthreshold swing, negative capacitance, In$_2$O$_3$, logic circuit

Due to their chemical stability, excellent crystallinity, and low-cost synthesis, metal oxide nanowires (NWs) can improve device performance through enhanced gate capacitance coupling. Thus, multiple electronic devices have been demonstrated based on one-dimensional (1D) semiconductor NWs, such as sensors, diodes, resistors, memory units, photodetectors, solar cells, and field-effect transistors (FETs). Among these metal oxide NWs, In$_2$O$_3$, with a high field-effect carrier mobility, wide band gap ($\sim 3.6$ eV), controllable electrical properties, and good metal–semiconductor contact, is a promising active material for integrated nanoscale electronics.

Meanwhile, with the ongoing scaling of FETs, it is very important to compress the power dissipation for all the switching issues. It is clear that the steep subthreshold characteristics indicate a low operation voltage and switching energy. However, the Boltzmann distribution prevents conventional MOSFETs from having an SS below 60 mV/dec at room temperature. Although transistors based on other operating principles, such as band-to-band tunneling and impact ionization, are proposed, these devices have been restricted from their compatibility or high operation voltages. Meanwhile, it seems that the use of negative capacitance, which is compatible with the current basic physics and...
standard microfabrication of MOSFETs, to solve this issue is more noteworthy. By replacing the conventional dielectric material with ferroelectrics, the change in channel surface potential can be more than that in the gate voltage, when the negative capacitance from the ferroelectrics is effectively stabilized. This "voltage amplification" effect has the potential to reduce the SS down to the sub-60 mV/dec regime.

Figure 1. Device structure, schematic illustrations, and electric performance of the side-gated steep slope FETs based on In$_2$O$_3$ NWs. (a) Device structure of the steep slope FETs, while (b) and (c) illustrate the on- and off-states, respectively, with opposing of electric fields in the P(VDF-TrFE) thin film. (d) False color SEM image of the measured steep slope FET; the scale bar is 4 μm. Parts (e) and (f) present the output and transfer characteristics, respectively, of the same device measured at room temperature. The inset in (e) illustrates the equivalent circuit for the capacitive voltage divider in the steep slope FETs. (g) The SS estimated from transfer characteristics versus the drain current, showing a sub-60 mV/dec SS.
Since the negative capacitance state is intrinsically unstable, efforts have been made to experimentally explore the negative capacitance effect.\textsuperscript{23,30–39} Although 2D materials have attracted researchers for their numerous advantages, the environment sensitivity and the interfacial effects often involve passivation layer deposition for a stable performance. Moreover, the non-dangling bonds also lead to the challenges for dielectric deposition.\textsuperscript{20,40} Hence, it is desirable to assemble steep slope FETs based on 1D metal oxide NWs with high performance and stability. Simpler device processing is better for low-cost, energy-saving, and high-efficiency technologies. However, due to the additional capacitor divider, all the reports solving the issue of "Boltzmann tyranny" complicate the device structures. Thus, there is significant room to experimentally investigate steep slope FETs, which are still in their early research phase.

In this work, In\textsubscript{2}O\textsubscript{3} NW transistors with sub-60 mV/dec SS are fabricated utilizing organic ferroelectric P(VDF-TrFE) as the gate insulator and assembled via spin coating. A side-gate structure is utilized to enable a simple approach, in which only one electron beam lithography (EBL) processing step is needed. The reported steep slope FETs present an \( \sim 10 \) mV/dec SS spanning over 5 orders of magnitude in the drain current at room temperature. The high on/off ratio of more than 10\(^8\) and a \( g_{m} \) of 2.3 \( \mu \)S are obtained simultaneously. In further testing for improved statistics, all the devices show sub-60 mV/dec SS. The improved SS is elucidated from a "voltage amplification" resulting from the effective negative capacitance, which is also confirmed by the negative drain-introduced barrier lowering (DIBL). When applied as inverters, the steep SS transistors lead to a voltage gain as high as 41.6, with NOR and NAND gates also being assembled. To functionize the steep slope FETs further, the Schmitt trigger inverters containing only one FET are demonstrated.

RESULTS AND DISCUSSION

Figure 1a demonstrates the device structure of the steep slope FETs with a spin-coated ferroelectric P(VDF-TrFE). The In\textsubscript{2}O\textsubscript{3} NWs, with a uniform radius of \( \sim 25 \) nm, were synthesized by a chemical vapor deposition (CVD) process and transferred subsequently onto a Si/SiO\textsubscript{2} substrate with a 100 nm-thick SiO\textsubscript{2} layer. The source, drain, and side-gate electrodes in this work were defined with only one EBL step, followed by the deposition of Cr/Au (10/50 nm) and a lift-off process. Then, the ferroelectric film was assembled by spin-coating to form a uniform thin film covering the entire substrate. Finally, the substrate with ready-made FETs was baked on a hot plate at 130 °C for 2 h. In general, a top-gate, multigate, or 3D-gate with ultrathin and high-\( k \) dielectric layer are utilized in other reports to improve the performance.\textsuperscript{25–35,41,42} In contrast, the fabrication process in this work has low cost and high efficiency.

The top schematic view of the device in this work is illustrated by Figure 1b,c. Figure S1a displays the XRD pattern of the baked P(VDF-TrFE) film with a character peak corresponding to the polar \( \beta \)-crystalline phase,\textsuperscript{43} which is necessary for negative capacitance. When in the on-state, as depicted in Figure 1b, there will be polarization pointing from the side gate to the In\textsubscript{2}O\textsubscript{3} NWs in the ferroelectric layer stemming from an applied fit positive voltage at the side gate. The polarization will accumulate electrons in the In\textsubscript{2}O\textsubscript{3} NWs. In the same way, after a fit negative gate voltage is applied, as seen in Figure 1c, the NW channel will be depleted, and the device will be in the off-state. Although the ferroelectric polarization is also useful in this work, the key operating principle is different from the conventional ferroelectric field-effect transistors (Fe-FETs) that depend only on the high-\( k \) and the remnant polarization of the ferroelectrics.\textsuperscript{1,20,44–48} The motivation here is to utilize the negative capacitance effect as a "voltage amplifier" to improve the SS, as revealed and explained in detail later.

The relevant SEM image shown in Figure 1d illustrates a top view of the measured FET. In the device, the channel length is designed to be 3 \( \mu \)m, and the width between the channel and the side gate is \( \sim 230 \) nm. Although there is an \( \sim 120 \) nm thick P(VDF-TrFE) film with a wave-like surface covering the device,\textsuperscript{1} the NW with an approximate diameter of 50 nm was obtained. Figure 1e,f shows the typical transfer and output characteristics of the device, respectively. The output characteristics suggests good ohmic contacts between the NWs and the electrodes, according to their liner behavior at a low drain bias. As depicted in Figure 1e, when the sweeping range of the gate voltage is \( \pm 10 \) V, the channel is depleted fully, and an on/off ratio of more than 10\(^7\) at room temperature is achieved. The results suggest that the conductivity of the In\textsubscript{2}O\textsubscript{3} channel can be controlled effectively when a suitable gate voltage is applied.

The traditional back-gated counterparts have an SS value of more than 150 mV/dec (Figure S2, with 100 nm SiO\textsubscript{2} as dielectrics), which agree with or are even smaller than the typically reported values.\textsuperscript{2,22} In contrast, the tested side-gated steep slope FET (Figure 1g) illustrates an SS <60 mV/dec and spanning over 4.5 orders of magnitude in \( I_{\text{on}} \) at room temperature and in ambient air. The smallest SS value is below 15 mV/dec, while no evidence of gate-induced leakage is observed. Although the lowest SS value of 80 mV/dec from forward sweeping is larger than that from reverse sweeping, there is a distinct superiority to the conventional counterparts, such as those given in Figure S2 and from other reports.\textsuperscript{2,22,49}

To compare the conventional MOSFETs and the steep slope FETs without the influence from the individuality of NWs, the P(VDF-TrFE) was spin-coated on the same device measured in Figure S2, and the relevant steep slope results are shown in Figure S3 revealing an SS value below 60 mV/dec Thus, it is suggested that the P(VDF-TrFE) dielectric layer can significantly improve the switching performance of the In\textsubscript{2}O\textsubscript{3} NW-based FETs and drive them toward theoretical limits. Furthermore, the enhancement from the additional back-gate voltage on the SS is also revealed. As illustrated in Figure S3c, because of the additional controls from the back gate, increasing the back-gate voltage from \( -15 \) to +15 V in 5 \( V \) steps causes the SS value to become smaller. This phenomenon indicates that the threshold voltage, SS, on/off ratio, and other performances of the steep slope FETs may be modulated with a piezoelectricity that avoids changing in instinct property of the channel or modifying the device parameters.

A statistical analysis of the SS value from 27 individual devices without additional back-gate voltage was also performed. Figure S4a shows that the lowest SS value is 11.3 mV/dec, and a sub-60 mV/dec SS is achieved for all the measured devices. According to Figure S4b, the average value of SS is calculated to be 28.94 mV/dec, and 37% of the measured devices demonstrate an extremely small SS of 14 ± 4 mV/dec The stability of the SS of <60 mV/dec from different devices is revealed from the above results and confirms the
ability of the ferroelectric layer to overcome the fundamental limits of the MOSFETs.

Figure 2a displays the transfer characteristics of four steep slope FETs with different P(VDF-TrFE) widths of 108.5, 137.8, 278.2, and 391.7 nm, which are based on the same NW (∼50 nm diameter) and the same channel length of 3 μm (Figure S5a). The relevant output characteristics of the four devices are shown in Figures S5b–e. As revealed in Figure 2b, all these devices achieve a sub-60 mV/dec SS spanning over 5 orders of magnitude in the Id, and the smallest SS is ∼10 mV/dec. Meanwhile, the high on/off ratio of more than 10^8 and a g_m of 2.3 μS are simultaneously obtained. When the width of the P(VDF-TrFE) decreases, SS values are constantly lower than 60 mV/dec, and the g_m and the V_{pinch-off} illustrate a trend of general improvement (Figure S5a). The relevant output characteristics of the four devices are shown in Figure S5a. As revealed in Figure 2b, all these devices achieve a sub-60 mV/dec SS spanning over 5 orders of magnitude in the Id, and the smallest SS is ∼10 mV/dec. Meanwhile, the high on/off ratio of more than 10^8 and a g_m of 2.3 μS are simultaneously obtained. When the width of the P(VDF-TrFE) decreases, SS values are constantly lower than 60 mV/dec, and the g_m and the V_{pinch-off} illustrate a trend of general improvement (Figure S5a). The relevant output characteristics of the four devices are shown in Figure S5a.

As is well-known, it is impractical for conventional MOSFETs to overcome the lower limit of the SS since the electrons follow a Boltzmann distribution. To understand the above results of an ultralow SS, it is necessary to explain the ability of a negative capacitance to overcome the “Boltzmann tyranny” through the “voltage amplification” resulting from the effective negative capacitance, which can be provided by replacing conventional dielectrics with ferroelectrics. The SS can be expressed by the equation SS = \frac{\partial \psi}{\partial \log Id} = \frac{\partial \psi_s}{\partial \log Id}, where V_g is the applied gate voltage, and \psi_s is the surface potential on the channel. Since the capacitance of the insulator and semiconductor is in series, as shown in the inset of Figure 1c, the \frac{\partial \psi_s}{\partial \log Id} term (often known

Figure 2. Electric measurements of the steep slope FETs with a sub-60 mV/dec SS at room temperature. (a) The transfer characteristics of the steep slope FETs with different P(VDF-TrFE) widths based on a single NW. (b and c) The SS estimated from the relevant transfer characteristics versus the drain current and P(VDF-TrFE) width, respectively. (d) The V_{pinch-off} and ΔV_h of the In2O3 FETs. (e) Transfer characteristics of another device showing a negative DIBL. (f) Relevant SS and V_{pinch-off}.
as the body factor "m") can be quantified by $\frac{\partial V}{\partial \Psi} = 1 + \frac{C_s}{C_{ins}}$. It is well-known that the $\frac{\partial V}{\partial \Psi}$ term is $\sim$60 mV/dec at room temperature, and due to the positive capacitances $C_{ins}$, the body factor "m" must exceed 1. The key function of ferroelectrics is to provide a negative value of $C_{ins}$ in the body factor "m", thus causing "m" to be less than 1. Consequently, the change in $\Psi$ can exceed the change in $V_g$, and this "voltage amplification" can enhance the SS to the sub-60 mV/dec regime. There is a caveat that the ferroelectric capacitor must be in series with a normal one (e.g., the $C_s$ in this work) so that the total capacitance is positive and the negative capacitance segment can be stabilized effectively, otherwise, the "voltage amplifier" will malfunction.34

Negative DIBL have been predicted and regarded as a phenomenon stemming from the negative capacitance effect in previous reports.26,50 As seen in Figure 2e, there are clear positive shifts in the reverse sweeping for the transfer characteristics of a device measured with $V_d$ from 0.1 to 1 V, and the $|V_{\text{pinch-off}}|$ shows an obvious decrease (Figure 2f). The negative DIBL is also observed in repeated measurements (Figure S7), from which it is revealed that although the transfer characteristics shift slightly to the right or left, a negative DIBL always appears during the reverse sweeping, corresponding with an ultralow SS (Figure S7d). This result confirms the effective negative capacitance from another perspective.

Then, the steep slope FET-based inverters were fabricated. The output and transfer characteristics of the FETs used to construct the inverter are illustrated in Figure 3a,b,
respectively. Figure 3c–f illustrates the static voltage transfer characteristic (VTC) curves of the inverter. The inverter contains one FET as a switch and one resistor as the load. When the FET is in the off-state, the voltage across the load will be very small due to the weak off-current in the channel, and the voltage across the FET ($V_{\text{out}}$) will be equal to the power supply $V_{\text{DD}}$. When the FET is in the on-state, $V_{\text{out}}$ will be close to 0 V resulting from the high conductivity of the FET. During the measurement, the side-gate voltage ($V_{\text{in}}$) was cycled between ±10 V to switch the FET between the on- and off-states. In this process, a voltage gain as high as 41.6 is obtained with a 500 MΩ load, as seen in Figure 3e. The results of the inverters with other load resistances are also displayed in Figures 3 and S9. Despite the relatively smaller voltage gains from forward sweeping, when considering that the load is a common resistor instead of carefully selected transistors that are usually utilized in other reports with high voltage gains, the results obtained in this work demonstrate the high performance of the steep slope FETs again.

The NAND and NOR gates were also assembled by utilizing the steep slope FETs. Figure 4a,b demonstrates the switching components of a NAND and a NOR gate constructed on single In$_2$O$_3$ NWs, respectively. Figure 4c shows the $V_{\text{out}}$ of a NAND gate depending on variations in the $V_{\text{in1}}$ and $V_{\text{in2}}$. The switching part of a NAND gate contains two FETs in series (inset of Figure 4c), with either or both inputs at the low potentials (e.g., −10 V) representing a logical 0, the output voltage will equal $V_{\text{DD}}$ (logical 1) due to the very low off-current of the FETs. The output voltage will be approximately 0 V (logical 0) when both FETs are turned into the on-state from the input at a high potential (e.g., +10 V), which is a logical 1. Distinct from the NAND gate, the switching part of a NOR gate consists of two FETs in parallel, as illustrated in the inset of Figure 4d. When either or both inputs are at high potentials (e.g., +10 V), representing a logical 1, the output voltage will be close to 0 V (logical 0) because of the high conductivity of the channel in the on-state. The output voltage will approximate the $V_{\text{DD}}$ (logical 1) when both FETs are

![Figure 4. Logic applications of the steep slope FETs. (a and b) Switching components in the NAND and NOR gates, respectively. (c and d) Output voltages of the NAND and NOR gates, respectively, depending on different inputs. (e–g) Transient response of the Schmitt trigger inverter under the triangular waveform input signals of (e) ±3 V at 0.05 Hz, (f) ±3 V at 0.1 Hz, and (g) ±2 V at 0.05 Hz.](image)
turned into the off-state from the input at a low potential (e.g., −10 V), which are logical 0.

The hysteresis loops observed in transfer characteristics of the steep slope FETs can simplify the Schmitt trigger inverters; thus, the circuits can be the same as the inverters that include only one FET (inset of Figure 3c), while the counterparts based on conventional MOSFETs usually require four to six transistors to construct the complex circuits. First, the fresh FET in the inverter was polarized with a triangular waveform input signal having an amplitude of ±10 V at 0.05 Hz (Figure S10a). Then, the amplitude of the input signal was decreased to ±3 V, as shown in Figure 4e, and the output voltage switched between 0 V and the V_DD of 5 V with a hysteresis of ~2 V, which is associated with the hysteresis characteristics of the steep slope FET. When the frequency of the input signal was raised to 0.1 Hz, there were no distortions in the output signal (Figure 4f). An applied input of ±2 V at 0.05 Hz gave similar results (Figure 4g). The input frequency was increased up to 1 Hz until distortions began to emerge (Figure S10b,c), due to the RC delays mainly stemming from the overlapping capacitances in the circuit. By assembling the Schmitt trigger inverters, the steep slope FETs are further functionalized.

A sub-60 mV/dec SS is achieved (measured V_d ≥ 0.1 V), and logic applications are demonstrated. However, there are many challenges remaining in this field. While the Schmitt trigger inverters are easily assembled due to the hysteresis in this work, this also indicates that sub-60 mV/dec SS and attractive hysteresis-free transfer characteristics cannot be achieved simultaneously. Hysteresis and sub-60 mV/dec SS often coexist in current reports. Furthermore, high-frequency performance still needs to be investigated to understand the details of the steep slope, and ferroelectric materials with short relaxation times for high-frequency operation are necessary to access practical applications.

CONCLUSIONS

In summary, the “Boltzmann tyranny” is overcome through a negative capacitance effect provided by a ferroelectric P(VDF-TrFE) insulator in side-gated In2O3 NW-based steep slope FETs. The FETs are designed to be side-gated to realize simple, low-cost, and high-efficiency fabrication using only one EBL step. These steep slope devices present better performances than conventional devices, including those employing multi- or 3D-gates with ultrathin and high-k dielectrics. The steep slope FETs in this report present sub-60 mV/dec SS spanning over 5 orders of magnitude in I_d. Moreover, a high on/off ratio of more than 10^6 and a g_m of 2.3 μS are obtained simultaneously at a V_d of 0.1 V. A statistical analysis was conducted, and all the measured FETs break through the physical limit of the SS. The average SS is estimated to be 28.94 mV/dec, and 37% of the steep slope FETs demonstrate extremely small SS of 14 ± 4 mV/dec or less, with the lowest SS of 11.3 mV/dec. The effective negative capacitance provided by the P(VDF-TrFE) accounts for the ultralow SS observed from the steep slope FETs. The mechanism can be understood from the “voltage amplification” function of the ferroelectric capacitor when the negative capacitance is effectively stabilized, and the effective negative capacitance is verified from the negative DIBL. Then, the steep slope FETs were employed to fabricate inverters with voltage gains as high as 41.6. In addition to the logic circuits of NOR and NAND gates, the Schmitt trigger inverters with the simplest circuit were also assembled to further demonstrate their logic applications.

METHODS

**FET Fabrication and Characterization.** In this report, the single crystalline In2O3 NWs utilized in the Schmitt trigger inverters were synthesized by a simple CVD method in a horizontal tube furnace. First, a quartz boat containing a mixture of In2O3 powder and graphite powder (10:1 weight ratio) was put in the tube furnace. Then, Si substrates with gold catalyst (1 nm thick) were placed in the downstream location of quartz tube that was ∼10 cm away from the evaporation source. Subsequently, the temperatures of the source and substrates were set at 1100 and 900 °C, respectively, and then heated continually for 1 h with a fixed current of argon/oxygen (100:1) gas at 200 sccm. When the reactor had cooled down, lots of NWs were formed on the Si substrates.

The XRD pattern and the PE-loop curve of the P(VDF-TrFE) thin film were measured by XRD on a Bruker D8 Advance diffractometer. The XRD pattern and the PE-loop curve of the P(VDF-TrFE) thin film were measured by XRD on a Bruker D8 Advance diffractometer. The PE-loop curve of the P(VDF-TrFE) thin film was measured by XRD on a Bruker D8 Advance diffractometer. The PE-loop curve of the P(VDF-TrFE) thin film was measured by XRD on a Bruker D8 Advance diffractometer. The PE-loop curve of the P(VDF-TrFE) thin film was measured by XRD on a Bruker D8 Advance diffractometer. The PE-loop curve of the P(VDF-TrFE) thin film was measured by XRD on a Bruker D8 Advance diffractometer.

**CONCLUSIONS**

In summary, the “Boltzmann tyranny” is overcome through a negative capacitance effect provided by a ferroelectric P(VDF-TrFE) insulator in side-gated In2O3 NW-based steep slope FETs. The FETs are designed to be side-gated to realize simple, low-cost, and high-efficiency fabrication using only one EBL step. These steep slope devices present better performances than conventional devices, including those employing multi- or 3D-gates with ultrathin and high-k dielectrics. The steep slope FETs in this report present sub-60 mV/dec SS spanning over 5 orders of magnitude in I_d. Moreover, a high on/off ratio of more than 10^6 and a g_m of 2.3 μS are obtained simultaneously at a V_d of 0.1 V. A statistical analysis was conducted, and all the measured FETs break through the physical limit of the SS. The average SS is estimated to be 28.94 mV/dec, and 37% of the steep slope FETs demonstrate extremely small SS of 14 ± 4 mV/dec or less, with the lowest SS of 11.3 mV/dec. The effective negative capacitance provided by the P(VDF-TrFE) accounts for the ultralow SS observed from the steep slope FETs. The mechanism can be understood from the “voltage amplification” function of the ferroelectric capacitor when the negative capacitance is effectively stabilized, and the effective negative capacitance is verified from the negative DIBL. Then, the steep slope FETs were employed to fabricate inverters with voltage gains as high as 41.6. In addition to the logic circuits of NOR and NAND gates, the Schmitt trigger inverters with the simplest circuit...
ACKNOWLEDGMENTS

The authors thank the support of national key R & D project from Minister of Science and Technology, China (2016YFA0220703), National Natural Science Foundation of China (nos. 61675027, 51622205, 51432005, 61505010, and 51502018), the support of national key R & D project from Minister of Science and Technology, China (2016YFA0220703), Beijing City Committee of science and technology (Z171100002017019), Beijing Natural Science Foundation (4181004, 4182080, 4184110, and 2184131) and the “Thousand Talents” program of China for pioneering researchers and innovative teams.

REFERENCES


