FULL PAPER

Performance Limits of the Self-Aligned Nanowire Top-Gated MoS_2 Transistors

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In order to realize the promising potential of MoS_2 as the alternative channel material, it is essential to achieve high-performance top-gated MoS_2 field-effect transistors (FETs), especially since the back-gated counterparts cannot control the device individually. Although uniform high-*k* dielectric films, such as HfO_2, can be obtained through the introduction of artificial nucleation sites on the MoS_2 channel to fabricate top-gated FETs, this would inevitably degrade their channel/dielectric interface quality, induce significant charged impurity scattering and lower carrier mobility. In this work, MoS_2 FETs are fabricated using a self-aligned nanowire top-gate, which can effectively reduce the charged impurity scattering on the surface of MoS_2. Specifically, the fabricated short-channel devices exhibit impressive electrical performances, such as the high on/off current ratio, low interface trap density, and near-ideal subthreshold slope at room temperature. In addition, the short channel effect is systematically analyzed, which indicates that the phonon scattering can be the dominant scattering mechanism in the devices when the amount of charged impurities is effectively reduced with the self-aligned nanowire gate. All these provide an enhanced fabrication scheme to attain top-gated short-channel devices with the optimized interface and potentially to explore their corresponding performance limits.

1. Introduction

MoS_2, as a 2D layered material, has attracted the most attention in the family of transition metal dichalcogenides (TMDs) due to its desirable properties for numerous electronic and optoelectronic applications.[1–10] As compared with the zero bandgap of graphene, MoS_2 exhibits a large bandgap ranging from 1.3 to 1.8 eV, simply depending on its different flake thicknesses,[11,12] which can facilitate its utilization in logic devices with a high on/off current ratio.[13–15] In addition, MoS_2 has also demonstrated with many other excellent characteristics, including the higher theoretical phonon-limited mobility,[16] respectable thermal stability[13,17] as well as good compatibility to silicon complementary metal oxide semiconductor (CMOS) processes.[7,8] Undoubtedly, MoS_2 could be considered as one of the most promising alternative channel materials for future field-effect transistors (FETs), especially since it is impractical to modify graphene with a sufficient bandgap similar to other semiconductors.

To explore TMDs, such as MoS_2, for the future electronic materials, there have been extensive amount of experimental and theoretical studies illustrated by many groups worldwide.[15,16,18,19] Among all the work, as back-gated transistors cannot control the individual operation of each MoS_2 device, it is important to fabricate high-performance top-gated MoS_2 FETs in order to enable their practical electronic applications in integrated logic circuits and others. However, this is always a well-known notorious challenge to obtain uniform thin-film dielectrics in the fabrication of top-gated MoS_2 devices because of the lacking of

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adequate dangling bonds on the surface of MoS_2 flakes.[13,20] If one would be able to deposit uniform high-k dielectric films on MoS_2 surface, sufficient nucleation sites must be artificially introduced onto the channel surface before or during the deposition. For example, one approach is known as the proper interface engineering by utilizing an ultrathin metal oxide (i.e., Y_2O_3) buffer layer, which can facilitate adequate nucleation sites, and then the subsequent uniform dielectric films can be deposited on the surface of MoS_2.[18] Nevertheless, this buffer layer would inevitably reduce the capacitance of the obtained top-gate dielectrics, along with the introduction of charged impurities contributing to the increased interface trap density (D_{it}) and the reduced carrier mobility (μ) of the MoS_2 channel. Another technique to attain uniform high-k dielectric films is the appropriate surface functionalization by using ozone or oxygen plasma pretreatment,[21,22] but this pretreatment would as well damage the surface of MoS_2, deteriorating the performance of fabricated MoS_2 FETs. In any case, even though the short channel effect is another significant issue that limits the device performance of short-channel MoS_2 FETs, only few work is performed to evaluate these effects.[15,23–26] Further understanding on the short channel effect of MoS_2 FETs configured in the top-gate geometry is still lacking, and it remains an unresolved challenge at this moment.

In this work, we fabricate short-channel MoS_2 FETs with a self-aligned nanowire top-gate. Specifically, the GaN nanowire is directly transferred onto the surface of MoS_2 through a physical assembly process at room temperature as the gate.[27–29] As compared with the atomic layer deposition (ALD) deposition of high-k dielectrics on the MoS_2 surface, this nanowire transfer process can reduce the number of charged impurities there. Because the atomically thin channels are very sensitive to the quality of both channel surfaces/interfaces,[30,31] so benefiting from this enhanced interface, all our devices exhibit the impressive electrical performance, including the high on/off current ratio of $>10^8$, minimal D_{it} down to 3.3×10^{11} cm^{-2} eV^{-1} and near-ideal subthreshold slope (SS) of 69 mV dec^{-1}. Moreover, a detailed analysis has also been carried out to assess the performance degradation resulting from the associated short channel effect of these devices. The saturation velocity (v_{sat}) of MoS_2 is found to be around 1.4×10^6 cm s^{-1} at room temperature while the relationship between the v_{sat} and the temperature in the short-channel device is evaluated and discussed thoroughly.

2. Results and Discussion

Figure 1a–c displays the schematic fabrication process of a MoS_2 FET configured with a self-aligned GaN nanowire top-gate. The few-layer MoS_2 flakes are first mechanically exfoliated from the MoS_2 crystal using the scotch tape technology and then transferred onto Si/SiO_2 (300 nm thick thermally grown oxide) substrates.[32,33] Here, the few-layer MoS_2 flakes are employed as the channel material because they can contribute to the higher current density and μ as contrasted to the single-layer MoS_2 counterpart, and at the same time to avoid degradation in the current on/off ratio and SS during the transistor design.[11,15] Afterward, the GaN nanowire is transferred onto the top of MoS_2 through a physical dry transfer process (Figure 1a).[27–29] The source, drain, and gate electrode are then one-off patterned by electron-beam lithography (EBL) and the electrodes (15/50 nm Ni/Au) are deposited by the use of thermal evaporation (Figure 1b). A thin metal layer (4/4 nm Ni/Au) is subsequently deposited onto the MoS_2 channel surface after the second EBL, in which it can naturally generate the short-channel device with a self-aligned nanowire top-gate geometry (Figure 1c). The cross-sectional schematic illustration of the fabricated device is depicted in Figure 1d while the corresponding atomic force microscope (AFM) and scanning electron microscope images are shown in Figure 1e and Figure S1(Supporting Information), respectively. It is noted that the GaN nanowire presented in this study is grown in a rectangular shape (Figure 1f), which allows seamless contact between the MoS_2 channel and the nanowire-gate, ensuring

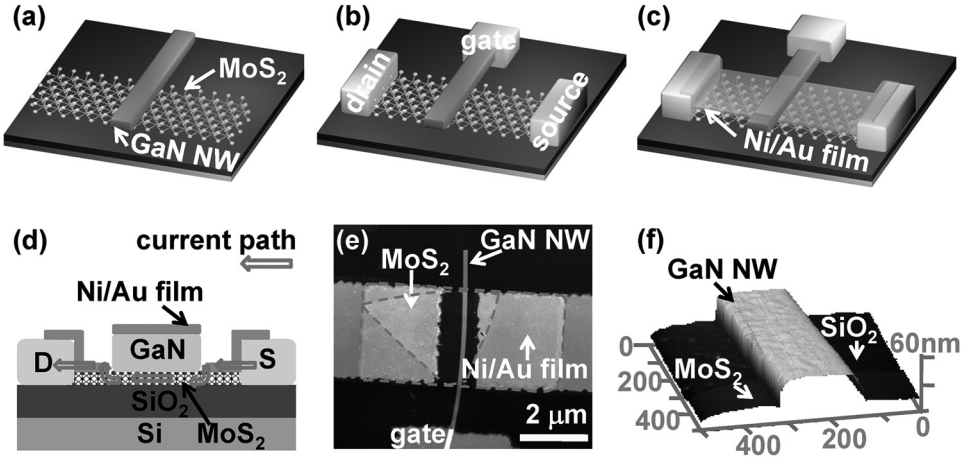

Figure 1. The fabrication process of the short-channel MoS_2 FETs with a self-aligned nanowire top-gate. a) The placement of the GaN nanowire top-gate onto the MoS_2 channel utilizing a self-aligned approach. b) The deposition of the source, drain, and gate electrodes. c) The deposition of a thin metal layer (4/4 nm Ni/Au) onto the channel of the MoS_2. d) The schematic diagram and e) its corresponding AFM image of the finished device. f) The AFM 3D-image of the GaN nanowire.

the excellent capacitive gate coupling for the enhanced device performance.[28] Because the GaN nanowire has a rectangular shape and a certain height so that the Ni/Au thin film will be split and discontinuous between the GaN nanowire and source/drain electrodes (Figure S2, Supporting Information).

In general, the GaN nanowires can be synthesized with different diameters through chemical vapor deposition (CVD) (Figure S3, Supporting Information), which are utilized to fabricate the top-gated MoS_2 FETs with different channel lengths. Before the deposition of thin metal films (4/4 nm Ni/Au) onto the surface of MoS_2 (**Figure 2**a; Figure S4, Supporting Information), the current–voltage (I–V) characteristics of both the GaN nanowire and MoS_2 are assessed, respectively, to evaluate their fundamental properties (Figure 2b). It is obvious that the GaN nanowire exhibits an acceptable conductivity such that it can be employed as the gate electrode of MoS_2 FETs. Moreover, the characteristic curve of the GaN/MoS_2 heterojunction is also measured in Figure 2c. The turn-on voltage is at around 3 V, indicating that there is a thin depletion region between the GaN nanowire and the MoS_2 channel. This is because the work function between them is different and the GaN nanowire synthesized by CVD is weak p-type in our work, which is similar to some other doping research,[34–37] as shown in Figure S5a (Supporting Information). The energy band diagram of GaN/MoS_2 heterojunction is also shown in Figure S5b (Supporting Information). The thin depletion region at the heterojunction can be used to restrain the charge leakage between GaN nanowire and MoS_2 channel, which is the equivalent of the Schottky barrier between metal and semiconductor in metal-semiconductor FETs (MESFET). This way, the GaN nanowire can be operated as an efficient top-gate of MoS_2 MESFETs with the minimal leakage current (Figure S6, Supporting Information). Then, the transfer characteristics of a representative MoS_2 MESFET before and after the deposition of thin metal films onto the MoS_2 channel are illustrated in Figure 2d. Although this device can be operated by tuning the nanowire top-gate bias and yielded a respectively high on-off current ratio, its output current is roughly one order of magnitude smaller than the one after the thin film deposition. This confirms that depositing the metal thin film onto the MoS_2 channel can effectively reduce the access resistance;[27,28] therefore, these metal films would be deposited onto all the devices studied in this work in order to explore the performance limits of the short-channel FETs. At the same time, the gate capacitance value is another important and necessary parameter for studying the short channel effect as well as other device properties. Given the structure of our MoS_2 FETs, the gate capacitance can be acquired from the transfer characteristics varied with applying different bottom-gate voltage (V_{bg}). As shown in Figure 2e, when the V_{bg} increases, it is clear that the transfer curves would shift to the left toward the negative bias. Notably, the slope associated with the plot of turn-on voltage ($V_{turn\text{-}on}$) as a function of V_{bg} (Figure 2f) is exactly equal to the ratio between the back-gate and top-gate capacitance (C_{bg} and C_{tg}).[28,38] The C_{bg} can be further calculated using the equation of $\varepsilon_0\varepsilon_r/d$, where ε_0 is the vacuum permittivity, d_{bg} = 300 nm and ε_r = 3.9 for SiO_2. In this case, utilizing the C_{bg} of 11.5 nF cm^{-2}, the C_{tg} of our MoS_2 FETs is found to be about 300 nF cm^{-2}.

As for a comparison, we also fabricate and measure a complete set of MoS_2 FETs with different channel lengths, which is achieved by varying the diameter of the GaN nanowire top-gate. Although other nanowire materials can as well be used as the top-gate (Figure S7, Supporting Information), the device demonstrates the best performance by tuning the GaN nanowire top-gate bias. All these devices are evaluated in vacuum environment in order to minimize any ambient effect for a

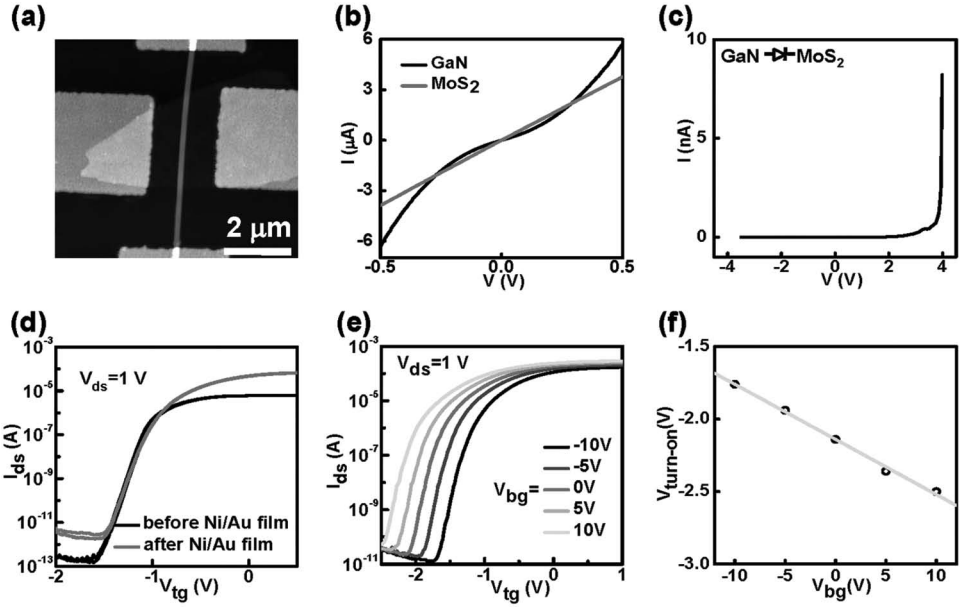

Figure 2. a) The AFM image before the deposition of a thin metal layer. b) I–V characteristics of the GaN nanowire and MoS_2 flake, respectively. c) The typical characteristic curve of the GaN/MoS_2 heterojunction measured. d) The transfer curve before and after the deposition of a thin metal layer. e) The shift of the transfer curves with increasing V_{bg}. f) The variation of the turn-on voltage ($V_{turn\text{-}on}$) at different V_{bg}.

consistent consideration. Among all the devices, transfer curves of the MoS_2 FET with the channel length of 230 nm are focused and measured at 0.01, 0.1, and 1 V, respectively, as depicted in **Figure 3**a. Given the shorter channel length than other reports, they display a remarkable switching behavior, such as the low off-state current (0.3 pA), high on/off current ratio (3×10^8) and excellent SS (69 mV dec^{-1}) at V_{ds} = 1 V.[15,18,21] The corresponding output curves are also shown in Figure 3b with a top-gate voltage sweeping from –1 to 1.5 V. It is worth noticing that there is an obvious drain current saturation in the output curves. Combining with the nearly linear drain current variation in the small source/drain bias range, all these indicate the good ohmic contact between the source/drain electrodes and the MoS_2 channel.[18,21] On the other hand, when the device channel length is shortened to 90 nm, there is a significant performance degradation due to the short channel effect as illustrated in Figure 3c,d. The current on/off ratio drops to 6×10^5 and the SS increases to 142 mV dec^{-1} at V_{ds} = 1 V. Meanwhile, the threshold voltage is shifted to the left toward the negative gate bias and the off-state current also increases substantially. All these would make the device less attractive for the practical utilization. Furthermore, a severe drain-induced barrier lowing (DIBL) is as well observed in Figure 3c. The DIBL is defined as the gate voltage shift (ΔV_{th}) divided by the drain voltage variation (ΔV_{ds}), where the ΔV_{th} is required for the fixed drain current density.[39–41] Hence, the DIBL effect can be calculated as the following

$$\mathrm{DIBL} = -\frac{\Delta V_{\mathrm{th}}}{\Delta V_{\mathrm{ds}}} = -\frac{V_{\mathrm{th}}\,|_{V_{\mathrm{ds}2}} - V_{\mathrm{th}}\,|_{V_{\mathrm{ds}1}}}{V_{\mathrm{ds}2} - V_{\mathrm{ds}1}} \tag{1}$$

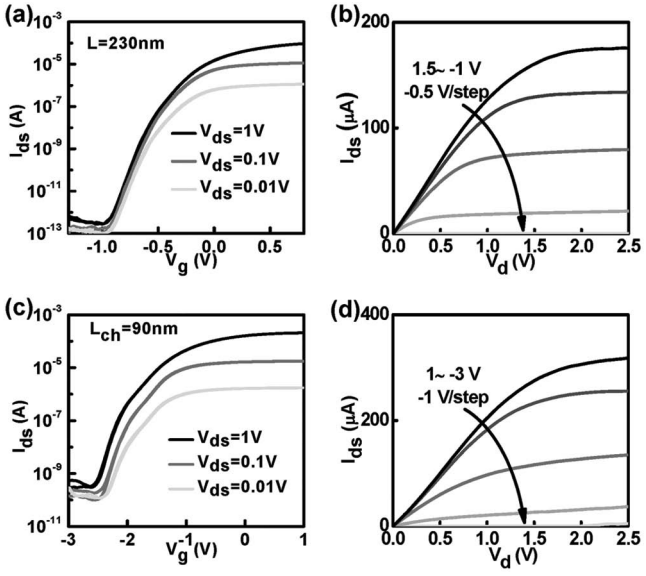

Figure 3. Transfer and output characteristics with different channel lengths. a) The transfer characteristics of a typical device with the 230 nm channel length at different drain voltages of 0.01, 0.1, 1 V. b) The corresponding output characteristics of the device with the 230 nm channel length. c) The transfer characteristics of a typical device with the 90 nm channel length at varied drain voltages of 0.01, 0.1, 1 V. d) The corresponding output characteristics of the device with the 90 nm channel length.

In specific, the drain current density is fixed to 10^{-2} μA $μm^{-1}$ in all our devices for the ΔV_{th} calculation. Then, the V_{ds2} and V_{ds1} are chosen as 1 and 0.1 V, respectively. Based on the formula (1), the DIBL is found to be 40.7 and 179 mV V^{-1} for devices with the channel length of 230 and 90 nm, accordingly. These DIBL values are much smaller than those previously reported,[15,24] which indicates that the short channel effects get suppressed in our MoS_2 FETs with a self-aligned nanowire top-gate. Although the barrier height at the source end is fixed for the long-channel devices, when the channel length continues to scale down, an increase of the drain bias can further induce the barrier lowering at the source end so that this DIBL effect is inescapable. More importantly, the barrier lowering would lead to the injection of extra carriers into the channel from the source to drain.[42] As a result, the performance degradation would appear as depicted in **Figure 4**a–d, and it would be even more challenging to obtain high-performance short-channel devices.

Moreover, it is noted that the hysteresis of the transfer curves is fairly small from different sweeping directions (Figure 3a and Figure 3c), which can be attributed to the excellent interface quality between the self-aligned nanowire top-gate and the MoS_2 surface.[42,43] In order to evaluate the interface quality, we employ the parameter of D_{it} based on the following equation[24,44,45]

$$\mathrm{ss}_{\min} = \frac{kT}{q}\ln(10)\left(1 + \frac{C_{\mathrm{dep}} + C_{\mathrm{it}}}{C_{\mathrm{ox}}}\right) \tag{2}$$

Here, q is the electron charge, k is Boltzmann's constant, T is the measurement temperature (300 K), C_{dep} is the depletion region capacitance, C_{ox} is the oxide capacitance of the top-gate, and C_{it} is the interface trap capacitance which can be defined as $D_{it} = C_{it}/q^2$. For ultrathin MoS_2 devices, it is assumed that the conducting channel is fully depleted, and

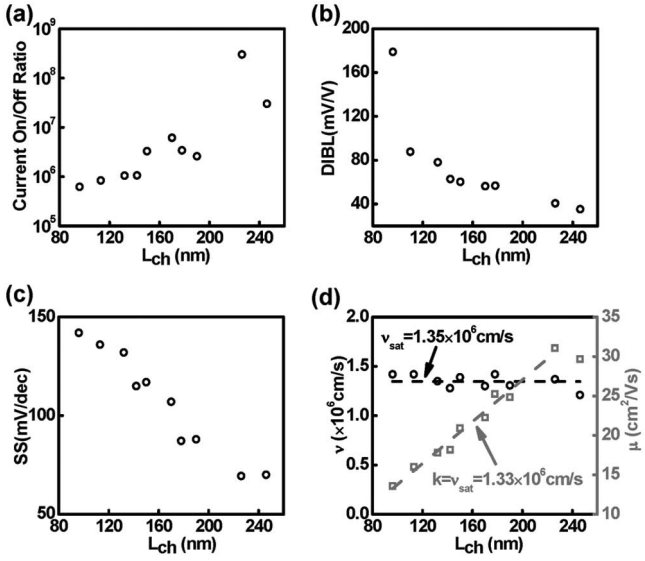

Figure 4. The changes of the device performance with decreasing channel length at V_{ds} = 1 V. The statistical data include a) current on–off ratio, b) the DIBL effect, c) the SS, and d) thev_{drift} and the μ.

hence C_{dep} can be considered as zero. According to the value of the C_{tg} in our devices, the C_{ox} is estimated to be about 300 nF cm^{-2}. Using Equation (2), the value of D_{it} can be extracted as 3.1×10^{11} cm^{-2} eV^{-1} for the device with 230 nm channel length, in which this D_{it} value is already about one order of magnitude smaller than those reported previously of directly depositing the uniform HfO_2 dielectrics onto the MoS_2 surface.[18,21] This points toward that an enhanced interface quality between the MoS_2 channel and the nanowire top-gate is obtained utilizing the current self-aligned nanowire assembly approach. This improvement is mainly due to the fact that it is not necessary for the self-aligned nanowire scheme to artificially introduce nucleation sites on MoS_2 as compared with the uniform HfO_2 deposition by ALD, in which those sites can be potentially contributed to the interface traps.

Apart from the discussion above, the drift velocity (v_{drift}) of carriers has as well an important influence on the carrier transport of FETs.[15,28,42] The v_{drift} can be calculated by this equation[18,27,28]

$$v_{drift} = \frac{L_{gate}}{\tau_t} = \frac{L_{gate} g_m}{C_{tg}} \quad (3)$$

where τ_t is the carrier transit time and it can be estimated by $\tau_t = C_{tg}/g_m$,[18,28] and $g_m = dI_{ds}/dV_{gs}$ represents the peak transconductance. Based on Equation (3), the v_{drift} of our devices is assessed and shown in Figure 4d with different channel lengths. Surprisingly, the v_{drift} is found to be nearly constant at 1.4×10^6 cm s^{-1}. According to the equation of $v_{drift} = \mu E$, at the low electric field, the μ is roughly constant and the v_{drift} should become larger with the reduction of the channel length because of the inverse proportional relationship between the electric field in the channel and the channel length. However, when the channel length is sufficiently short, the v_{drift} would approach the saturation, v_{sat}, and it would maintain a constant value there. At the high electric field, it leads to the decrement of μ with scaling down the channel length.[15,26,42] In this case, the v_{drift} is consistent with the v_{sat} in our short-channel devices; therefore, the value of the v_{sat} can be confirmed at about 1.4×10^6 cm s^{-1}, which is similar to the previous studies.[18,27,46] In order to verify the relationship between the v_{sat} and the μ in our short-channel devices, μ is extracted using the equation

$$\mu = \frac{1}{C_{tg}} \frac{L}{W} \frac{g_m}{V_{ds}} \quad (4)$$

It is clear that μ is decreased with the reducing channel length of our devices (Figure 4d). Based on the equation of $v_{drift} = \mu E = \mu V_{ds}/L$, the v_{sat} can as well be pull out from the slope of the plot between the μ and the channel length at the high electric field. This way, the v_{sat} of 1.3×10^6 cm s^{-1} can be directly obtained from the slope in Figure 4d, which is consistent to the previously reported values within the range of error allowed. All these results demonstrate the validity of our findings regarding the device property changes with the scaled channel length.

To further shed light into the carrier transport of our short-channel devices, as depicted in **Figure 5**a, the corresponding transfer characteristics are considered and evaluated with variable temperatures down to 77 K. As the hysteresis of the transfer curves is fairly small from different sweeping directions, results presented with the sweeping direction from the negative to positive voltages are included here. Figure 5b demonstrates that the SS and the turn-on voltage get improved with the decreasing temperature because of the Arrhenius relationship between the SS and the temperature such that $SS_{min} \approx \ln(10)kT/q$.[47] More importantly, the μ and the v_{sat} are also found to be enhanced with the decreasing temperature as shown in Figure 5c. When the temperature is reduced to 77 K, the μ and the v_{sat} would reach the values of 47.6 cm^2 V^{-1} s^{-1} and 2.1×10^6 cm s^{-1}, respectively, for the device with the channel length of 230 nm due to the vital roles of various scattering mechanisms, which affect the carrier transport here.[48] Among various mechanisms, the two most important scattering events are the phonon and impurity scattering. The phonon scattering would decrease with the reduction of the lattice vibration, which results from the temperature reduction. Since it is confirmed that there is fewer charged impurities associated with the impressively low D_{it} values for our devices, the impact coming from impurity scattering can be assumed insignificant here. As a result, the μ and the v_{sat} variation with temperature can be affirmed from the effect of photon scattering.[25]

3. Conclusion

In summary, we fabricate MoS_2 FETs with different channel lengths down to 90 nm employing a self-aligned GaN nanowire top-gate configuration. Due to the excellent interface quality between the top-gate and the MoS_2 channel, our devices exhibit the superior electrical performance, such as the extremely

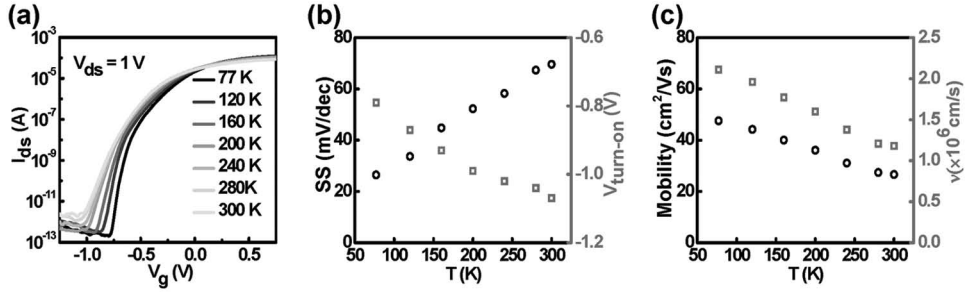

Figure 5. a) The transfer characteristics of our device measured with variable temperatures down to 77 K at V_{ds} = 1 V. b) The changes of SS and $V_{turn-on}$ with different temperatures. c) The changes of v_{drift} and the μ with different temperatures.

high on/off current ratio, near-ideal SS, and low D_{it}. In addition, we systematically investigate the short channel effect of these devices. The saturation velocity (v_{sat}) is found to be near 1.4×10^6 cm s^{-1} at room temperature, which is independent of the channel length, confirming the decisive role to the μ in these short-channel devices. All these results can enable us to obtain a comprehensive understanding about the performance limits in these top-gated short-channel MoS_2 FETs and provide an enhanced fabrication scheme to achieve high-performance devices with the optimized interface.

4. Experimental Section

Materials: The few-layer MoS_2 flakes were mechanically exfoliated from MoS_2 crystal purchased from SPI supplies using the scotch tape technology and then transferred onto Si/SiO_2 (300 nm thick thermally grown oxide) substrates. Also, GaN nanowires with different diameters were synthesized through the conventional CVD.

Device Fabrication and Measurements: The GaN nanowire was transferred onto the top surface of MoS_2 by the physical assembly process. Then, methyl methacrylate (MMA) and polymethyl methacrylate (PMMA) were spin-coated on the substrate and the e-beam lithography was used to define the source, drain, and gate patterns. The Ni/Au (15 nm/50 nm) electrodes were deposited by thermal evaporation and the acetone was used to lift-off the patterns. After that, a thin metal layer (4/4 nm Ni/Au) was deposited onto the surface of MoS_2 channel with the pattern created by the second lithographic process. The device was then finished with the final lift-off process. The transfer and output curves were all measured by the Lake Shore TTPX Probe Station and Agilent Semiconductor Parameter Analyzer at room temperature and low temperatures.

AFM Characterization: AFM imaging was obtained by Bruker Multimode 8 with Scan Assist-Air probe under peak force mode in the ambient condition.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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