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Article

Investigating the interlayer electron transport and its influence on the whole electric properties of black phosphorus

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ABSTRACT

Two-dimensional (2D) nanomaterials have attracted great attention in next generation electronic and optoelectronic technologies due to the unique layered structure and excellent physical and chemical properties. However, the mechanism of transmission along the vertical direction of 2D semiconductor materials has not been investigated. Here, we use first-principles calculations to explore the bandgap energies along different directions, and fabricate a vertical, a lateral and a mixture-structured black phosphorus field effect transistor (BPFET) to study the electrical characteristics along different directions under variable temperatures. The variable temperature test indicates that the mixture-structured device performs more like a lateral device, while the conductance along the vertical direction is hard to be tuned by temperature and electrical field. The unchanged conductance under electric field and variable temperatures allows the vertical device to act as a fixed resistor, promising possible application for the prospective electronic and optoelectronic devices.

1. Introduction

Two-dimensional (2D) nanomaterials such as graphene [1,2], transition metal dichalcogenides (TMDs) [3–10], black phosphorus (BP) [11,12], boron nitride (h-BN) [13,14], have attracted great attention as foundation blocks for next generation electronic and optoelectronic devices because of their unique layered structures, excellent physical and chemical properties [15]. Compared with conventional bulk materials, the layers of 2D materials are connected by van der Waals force instead of covalent bond, which leads to fewer dangling bonds and defects on the materials surface [8,16–18]. The layered structure makes it possible to reduce the thickness of 2D materials to monoatomic layer while maintain its crystal periodicity. Many novel physical phenomena have been discovered in monolayer/few layer materials with large lateral size [19–23]. Meanwhile, the bandgap of most 2D semiconductor materials can be easily tuned by simply changing the thickness [17]. Their controllable structure and unique properties make 2D semiconductor materials very promising for next generation electronic and optoelectronic applications. Most recently, many researches have been developed to study the electronic and optoelectronic properties of 2D materials, like graphene, MoS_2, WS_2, BP, etc. [12,24–28]. High carrier mobility and on/off ratio, excellent photosensitivity, and good infrared performance have been detected in these materials.

Up to now, almost all of the researches focus on investigating the performance of 2D materials along the lateral direction, while the (opto)electronic properties along the vertical direction remain to be revealed [17,29–31]. Recently, directional transfer technology have been employed to construct a vertical heterojunction by different 2D materials, and the interface in the vertical heterojunction was found to have a great influence on the (opto)electronic characteristics of the structure [32–36]. For example, Yu and co-workers [27] have fabricated a vertically stacked multi-heterostructures based on graphene and MoS_2 and found the vertical heterostructure integrated by layered materials can enable a new transistor simultaneously with high on/off ratio and high current density under room temperature, and the high performance electronic properties were caused by the changeable schottky barriers which can be tuned by the gate voltage. Along the lateral direction, the

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electrons transmit according to drifting motion under external energy and diffusion motion caused by thermal excitation. Nevertheless, the van der Waals force between layers and extremely short thickness make the electron transport along the vertical direction substantially different from the horizontal direction. The clarification of the behavior of electrons transport along the vertical direction may provide a new insight for next generation short channel devices.

In this work, we choose bipolar layered material BP to explore the mechanism of interlayer transmission of 2D materials. By using density functional theory (DFT) calculations, the bandgap energies of different directions were calculated. A vertical, a lateral and a mixture-structured black phosphorus field effect transistor (BPFET) were fabricated. The vertical BPFET has no semiconductor regulation performance even after the temperature was decreased to 10 K, nor the conductance and on/off ratio change under a strong electric field. Meanwhile, the mixture-structured BPFET mainly exhibits the characteristics of the lateral structure. The results indicate that BP shows no semiconductor characteristic along the vertical direction, but performs more like a resistor. We assume that this phenomenon may be caused by ultrafast electrons transport within layers and the fixed resistance between layers which remain unchanged with electric field and temperature. The work shed fundamental lights on unveiling the charge carrier transport behavior of 2D materials as well as offer useful guide for the fabricating of 2D electronic devices.

2. Experimental

2.1. Density functional theory calculation

The DFT calculations are performed using the VASP code with the projector augmented wave (PAW) potentials [37]. Perdew-Burke-Ernzerhof (PBE) scheme in the generalized gradient approximation (GGA) was used to treat the exchange-correlation energy [38]. The kinetic energy cutoff for the plane-wave basis set was 450 eV. The Brillouin zone was sampled with the Monkhorst-Pack k-point mesh with $8 \times 6 \times 2$. The ions were relaxed until the maximum forces were less than 0.03 eV/Å and the total energy was converged to 1×10^{-5} eV/atom. Because the weak chemical bonding between the structures of black phosphorus, a damped van der Waals (optB86b-vdW functional) correction was employed.

2.2. Device fabrication and measurement

Firstly, ultraviolet radiation photolithographic method was used to manufacture the lines on 300 nm thick SiO_2 on Si substrate. Next, 5 nm/15 nm Cr/Au was deposited as the down electrode. Compared with the custom thick electrodes, the extremely thin electrodes can avoid the change of electronic properties caused by the deformation of the BP flakes. Then, the BP nanoflakes purchased from HQ Graphene Company were mechanically exfoliated on the down electrodes. To separate the top electrodes from the down electrodes, a 40 nm thick Al_2O_3 was deposited on the BP flakes with atomic layer deposition (ALD) after micro patterning by using electron beam lithography. Finally, electron beam lithography was used to pattern the top electrodes, and 10 nm/50 nm Cr/Au was deposited as the top electrodes. The electrical characteristic was carried out by Keithley 4200, and a vacuum probing station was used for the high vacuum measurement. A temperature-changeable measurement system was employed to test the properties at different temperatures, with liquid helium acting as the coolant.

3. Results and discussion

To theoretically understand the interlayer electrons transport mechanism, we used first-principles calculations to explore the bandgap energies along different directions. Using VASP codes with projector augmented wave potentials, we obtained the bandgap energies of electron transition along [1 0 0], [0 1 0] and [0 0 1] directions of black phosphorus. Fig. 1a shows the atomic structures of black phosphorus, with [1 0 0], [0 0 1] and [0 1 0] representing the crystal structure along zigzag, armchair and vertical direction, respectively. The optical absorption near the band edge follows the formula of $\alpha h\nu = A(h\nu - E_g)^{1/2}$ for a semiconductor with direct, optically-allowed bandgap. A is a constant independent on the materials, and E_g represents the bandgap of the materials. The plot of $(\alpha h\nu)^2$ versus the photon energy $(h\nu)$ along three directions is shown in Fig. 1b. The estimated band gap energies along [1 0 0], [0 0 1] and [0 1 0] directions were about 2.1, 0.3 and 1.8 eV, respectively. The anisotropic character of bandgap energies will cause the optic and electronic anisotropy. The calculated bandgap energy along the lateral direction [0 0 1] is corresponding to the well-researched value for the bulk black phosphorus. Interestingly, we can find that the bandgap energy along the vertical direction [0 1 0] is 1.8 eV, a typical semiconductor character. This value represents that the electronic and optic properties along the [0 1 0] direction could be tuned by an external potential field, like electrical field or optic field.

The schematic vertical BP device is shown in Fig. 2a. Ultraviolet radiation photolithographic methods and electron beam lithography were used to pattern the electrodes and dielectric layer. The BP flake used in this research was deposited on Si wafer with 300 nm SiO_2 on its surface by mechanical exfoliation from a bulk BP crystal. Typical optical image of the device is shown in Fig. 2b. The channel is constituted by the BP flake, and the thickness of the BP flake is about 25 nm. Especially, the Al_2O_3 square acts as an insulating layer, which will prevent the electrons from transporting along the lateral direction. As shown in the Raman spectra in Fig. 2c, the characteristic vibration modes A_g^1, B_{2g} and A_g^2 of BP and the characteristic vibration modes of Si are clearly visible at 362, 439, 467 and 520.3 cm^{-1}, respectively.

Next, a lateral BP FET device and a vertical BP device were fabricated for comparison to investigate the transport properties. Considering the instability of BP flake under ambient environment, the measurements were taken under high vacuum environment (under 10^{-4} Pa) at room temperature (300 K). Schematic images of the lateral and vertical devices are shown in Fig. 3a and d, respectively. A conventional gate voltage was employed to regulate the carrier density of the devices. The arrows in the schematic images show the direction of the electric field lines under a negative gate voltage. For the lateral device, when a negative voltage was applied between the source electrode and gate electrode, the SiO_2 dielectric layer would be polarized, and then the positive charges would assemble on the top surface of the dielectric layer. When the gate voltage changed from a negative value to a positive one, the electric field would change from downward direction to upward, and the hole carrier density would decline gradually, leading to the variation of the conductance of the device. For the vertical device, due to the source electrode below the BP flake, the electric field lines would bend because of the electromagnetic shielding effect, as schematically shown in Fig. 3d, and the hole carrier density would also have a variation as the gate voltage changed. Fig. 3b shows the transfer characteristics of drain-source current I_{ds} and gate-source voltage V_g for the lateral device. It is obvious that the BP flake displays a p-type semiconducting behavior in our devices under room temperature. The semi-logarithmic transfer curve shows that the lateral device exhibits

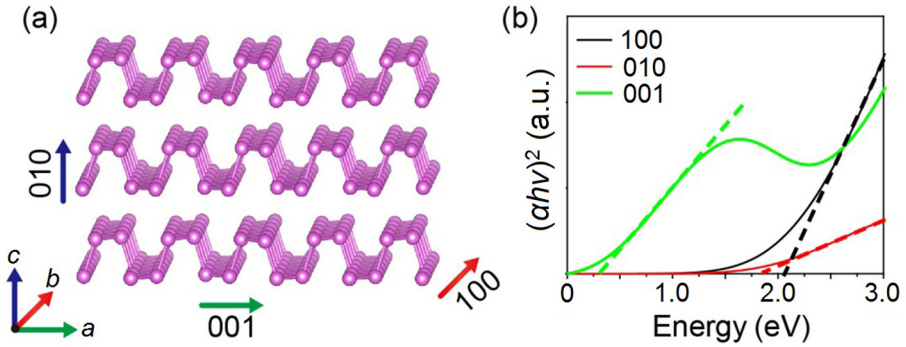

Fig. 1. (Color online) Density functional theory calculations results. (a) Atomic structures of black phosphorus; (b) bandgap energies along different directions.

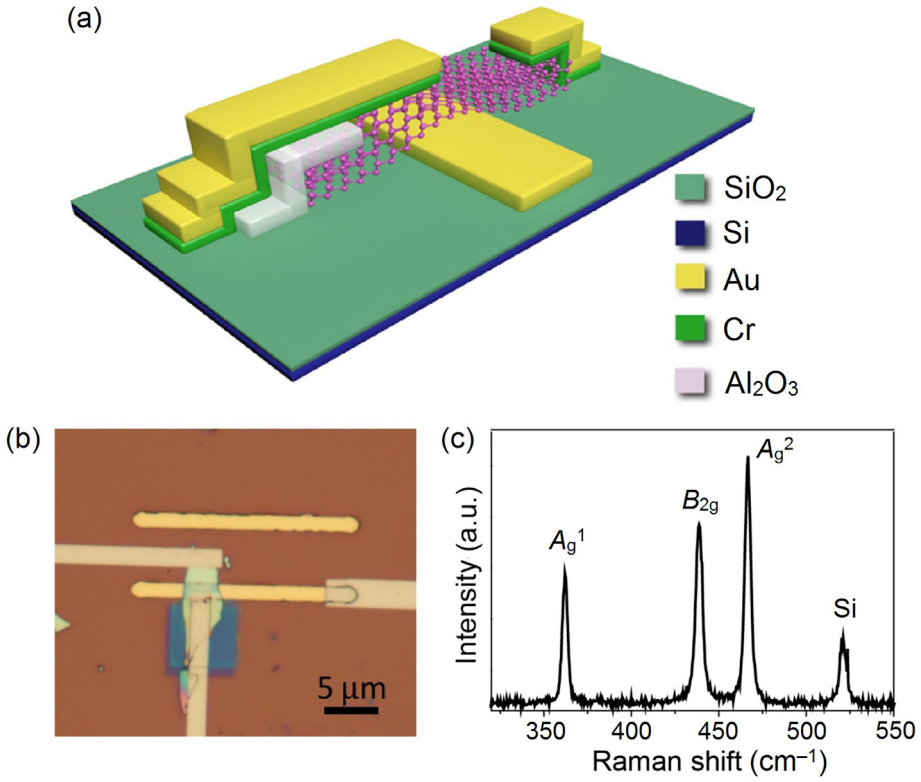

Fig. 2. (Color online) Schematic and optical images of the vertical BP devices. (a) Schematic image of the vertical device, with the different color squares at the bottom right corners representing different materials. (b) Typical optical image of a vertical BP device; the scale bar is 5 μm. (c) Raman spectrum of BP flake; Si Raman peak is indicated.

a high on/off current ratio of 10^2, and from the linear transfer curve, the maximum transconductance of the device is calculated to be 159.86 nS. The transconductance is defined by the formula, $g_m = \frac{dI_{ds}}{dV_g}$, which represents the characteristic of regulatory capacity of I_{ds} versus V_g. Nice linear relationship between I_{ds} and V_{ds} is observed under different gate voltages (V_g) bias, indicating the Ohmic contact characteristics between BP flake and Cr/Au electrodes, as shown in Fig. 3c. Fig. 3e shows the transfer characteristics of drain-source current I_{ds} and gate-source voltage V_g for the vertical device. Considering the extremely short channel (25 nm) between drain electrode and source electrode, the value of the V_{ds} is set to 5 mV to prevent the device from breakdown by a high electrical field. Compared to the lateral one, the vertical device displays an on/off current ratio smaller than 2, and the device still shows the properties of p-type semiconductor, and the transconductance of the device is only 1.22 nS. The small on/off ratio and small transconductance indicate that the resistance of the vertical device is hard to be tuned by gate voltage. Fig. 3f displays the output characteristics of the vertical device. Similar to the lateral device, the $I_{ds}-V_{ds}$ curves have well defined linear regimes, indicating the Ohmic contacts between the electrodes and BP flake.

Comparing the lateral and vertical devices, we found that there were all Ohmic contact between BP flake and electrodes, but the on/off ratio of the vertical device was extremely smaller than that of the lateral one. To uncover the mechanism for the great difference, low-temperature test was carried out. As we all know, the electric properties of BP flakes are sensitive to temperature, and the influence of electron scattering, interface defects, and surface defects will be suppressed at low temperature. Fig. 4a shows the typical p-type semiconducting transport characteristics of the lateral device under 10 K. Compared with 300 K, the regulatory capacity of the lateral device was greatly enhanced. The on/off ratio

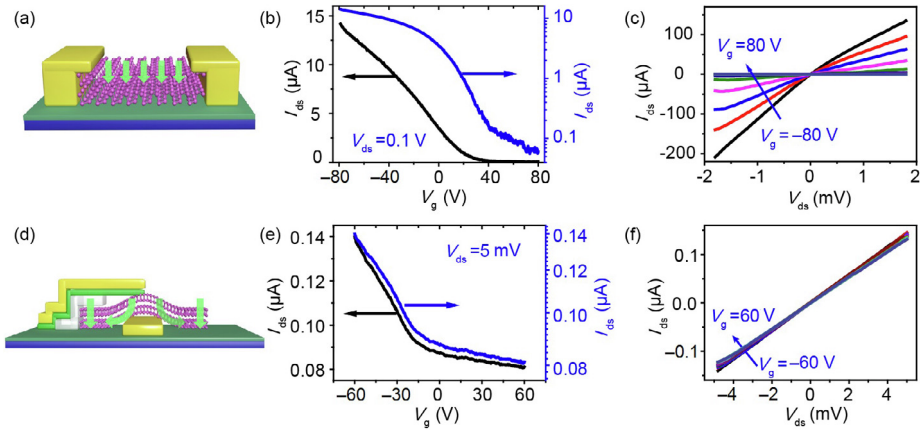

Fig. 3. (Color online) Schematic images and electric properties of lateral and vertical devices under high vacuum at room temperature. (a) Schematic image of the lateral device under a negative gate voltage; the arrow indicates the electric field lines. (b) Transfer characteristics of the lateral device on semi-logarithmic (blue) and linear (black) scales at a drain-source voltage bias of 100 mV. (c) Output characteristics of lateral device for V_{ds} sweeping from −2 to 2 V at V_g changes from −80 to 80 V in steps of 10 V. (d) Schematic image of the vertical device under a negative gate voltage. (e) Transfer characteristics of the vertical device on semi-logarithmic (blue) and linear (black) scales at a voltage bias of 5 mV between the drain and source electrode. (f) Current versus bias voltage (I_{ds}−V_{ds}) characteristics of vertical device for V_g changes from −60 to 60 V in steps of 10 V.

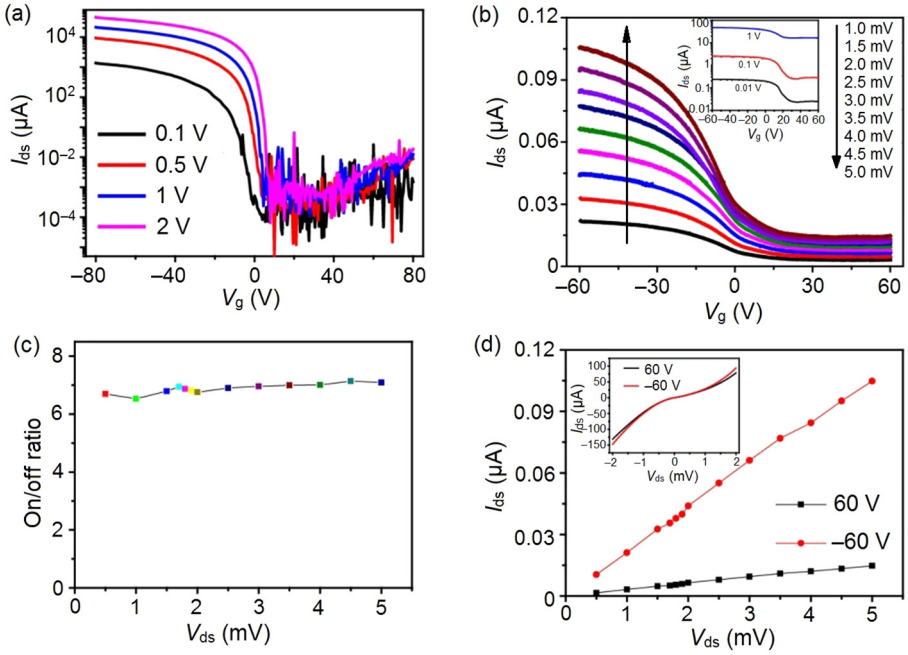

Fig. 4. (Color online) Electric properties of lateral and vertical devices at 10 K. (a) Transfer characteristics on semi-logarithmic scales of lateral device at V_{ds} of 0.1, 0.5, 1, and 2 V. (b) Transfer characteristics on linear scales of vertical device at V_{ds} varying from 1 to 5 mV, in steps of 0.5 mV; the inset figure shows the I_{ds}−V_g curves of 0.01, 0.1 and 1 V. (c) On/off ratio of vertical device under different drain source voltage bias. (d) I_{ds}−V_{ds} curves at small voltage bias under −60 and 60 V gate voltage; inset shows the curves at a large-scale voltage bias.

of the device increases to more than 10^6, the off current is smaller than 10^{-10}, and the device maintains an excellent tuning ability even if the electric field increases 20 times. The conductance (σ) of the lateral device consists of two parts, $\sigma = \sigma_{th} + \sigma_{ch}$ [39]. Here, σ_{th} is the contribution from all thermally activated charge carriers, which is determined by the temperature only. σ_{ch} is the conductance of the BP flake channel. For the lateral device, σ_{ch} is contributed by two parts: the top layer conduction, σ_{top}, which cannot be tuned by gate voltage due to electromagnetic screening, and the bottom layer conduction, σ_{bot}, which can be tuned by the gate voltage. In Drude model, $\sigma_{top(bot)} = n_{top(bot)} e \mu_{top(bot)}$, where $n_{top(bot)}$ and $\mu_{top(bot)}$ are the concentration and mobility of the free carriers, respectively, in the top (bottom) layer. The free carrier concentration of the top (bottom) layer is determined by temperature. As temperature decreases, the thickness of the bottom layer will increase, thus the charge carrier concentration of the bottom layer will increase, while that in the top layer will decrease. Meanwhile, the thermal conductance will decrease gradually due to the reduction of thermal emission. For a 25 nm thickness BP flake, when the temperature decreases to 10 K, all of the BP flake will be tuned by the gate voltage, and the conductance can be simplified as $\sigma_{th} + \sigma_{bot}$. When V_g transfers from negative to positive, σ_{bot} changes from a huge value to a small one. Therefore, the device shows an excellent tunability under 10 K temperature, as the conductance of the device is defined as the ratio of I_{ds} vs. V_{ds}, $\sigma = \frac{dI_{ds}}{dV_{ds}}$. When the gate voltage changes to 80 V bias, the conductance of the device is smaller than 10^{-9} S under 10 K.

The vertical device was also tested at low temperature. Fig. 4b reveals the electric properties of the device under different V_{ds} at 10 K. It is observed that the regulatory capacity of the device has a slight enhancement in comparison with that tested at 300 K. The on/off ratio of the device increases from 2 to 7 as temperature decreases from 300 to 10 K. Considering the vertical structure, the thermal conductance σ_{th} is similar to the lateral device, and σ_{ch} is the conductance of the BP flake along the vertical direction. For V_{ds} = 5 mV, when V_g varies from −60 to 60 V, the conductance changes from 2.05 to 0.402 mS. Compared to lateral device, the change is very tiny, and the variation is similar when V_{ds} changes from 1 mV to 1 V. This result manifests that the conductance of BP channel in vertical device maintains a constant value under 10 K temperature, and the conductance cannot be tuned by the external electric field. In Fig. S1 (online), the MoS_2 vertical device possesses the similar properties under low temperature. With temperature decreasing to 10 K, the MoS_2 vertical device exhibits a weak regulatory capacity and low on/off ratio, similar to the BP vertical device. Fig. 4c provides the on/off ratio at different V_{ds}, which obviously shows that the on/off ratio maintains at 7 when V_{ds} changes from 1 to 5 mV. This result indicates that the regulatory capacity of the device has a tiny variation under different V_{ds}. The I_{ds}-V_{ds} curve of vertical device under different gate voltage is shown in Fig. 4d, and the inset figure provides the I_{ds}-V_{ds} curve at a large range V_{ds} bias. For small bias voltage, the drain-source current under −60 and 60 V bias gate voltage varies linearly with the voltage, indicating that the contacts between BP flake and electrode under different V_g are all Ohmic contacts, whereas, the large bias voltage brings a nonlinear relationship. Considering the contact metals of top electrode and bottom electrode are Au and Cr, the nonlinear phenomenon may be caused by the different work functions of two different metals.

To sum up, the low temperature test shows that the transport mechanism of vertical device is different from the lateral device. The conductance of vertical device is very hard to be tuned under low temperature, and maintains a constant value under different gate voltages. To explore whether interlayer electrons transport can influence intralayer electric properties, a mixture-structured device is fabricated as shown schematically in Fig. 5a. The variable temperature transport characteristics of the vertical, lateral and mixture-structured devices are revealed in Fig. 5b–d, respectively. As shown in Fig. 5b, the regulatory capacity of vertical device almost has no change under different temperatures with the on/off ratio of the device maintaining at a fixed value. This result demonstrates that the conductance along the vertical direction remains unchanged in a broad range of ambient temperature. However, in Fig. 5c we can find that the on/off ratio of the lateral device gradually diminishes as temperature increases, and the conduction type varies from bipolar to p-type. As temperature increases, the thermal excitation becomes intense, leading to the enlargement of the thermal excitation conductance and the decrease of the bottom layer thickness. As a result, the regulatory capacity of the device becomes worse as temperatures increases. The electric transport characteristics of mixture-structured device under different temperatures are shown in Fig. 5d. Comparing the three curves, we can find that the electric property of the mixture-structured device is approaching to the lateral one. The variation of on/off ratio with temperature, conduction type, and regulatory capacity is similar to the lateral one, which indicates that electrons prefer to transport along the lateral direction, while the conductance along the vertical direction has little influence on the electric properties of the mixture-structured device. For the lateral device, when the electrical field is about 1 V/μm or lower, the drift-diffusion mechanism plays a vital role in the carrier transport. As a result, the electrical characteristic, such as the conductance, on/off ratio and transconductance, is sensitive to the temperature. On the contrary, for the vertical device as shown in Fig. 4b, when drain-source voltage increases from 1 mV to 1 V, the electrical intensity increases from 0.4 to 40 V/μm, whereas, the electrical properties almost have no change. In the drift-diffusion model, the Zener breakdown will lead to a weak regulatory capacity under 40 V/μm because of the high-field effect. Usually, the common device will be hard to reach saturation; however, the vertical device displays an obvious saturation region under a higher

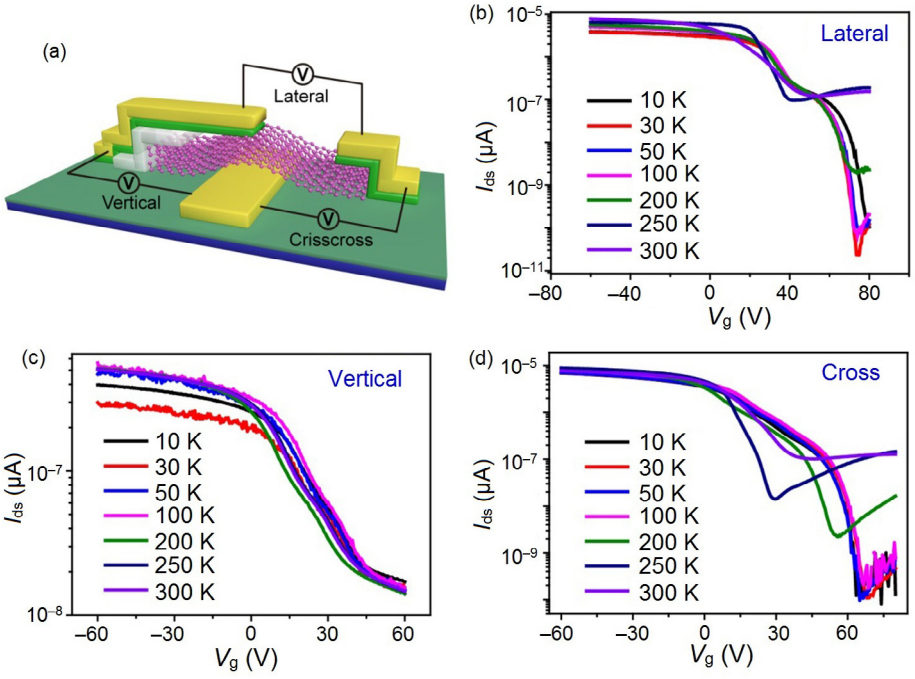

Fig. 5. (Color online) Transport characteristics of mixture-structured device under variable temperatures. (a) Schematic image of the mixture-structured device. Transfer characteristics of vertical device (b), structure device (c), and mixture-structured device (d).

negative (positive) gate voltage bias. This indicates that drift-diffusion model is not suitable for the carrier transport along the vertical direction. Considering the extremely short channel (25 nm) of the vertical device, we further explore the transport characteristics of the vertical device under a tiny V_{ds} bias, as shown in Fig. S2 (online). The transport properties of the device almost have no change for V_{ds} changes from 20 μV to 1 V, further confirming that negative differential resistance effect has not be found in the output characteristics of the vertical device, similar with results in Fig. 4b. All these results indicate that the tunneling effect takes no action in the vertical device. Thus we assume that the transport mechanism along the vertical direction may be ultrafast intralayer electrons transport, leading to the weak regulatory capacity and insensitive conductance to temperature. This mechanism gives rise to the fixed resistance along the vertical direction, and makes the electrical characteristics of the mixture-structured device display more like the lateral device.

4. Conclusion

In this work, we explored the electrons transport behavior along the lateral and vertical direction. The DFT calculations demonstrated that the bandgap energy along the vertical direction is 1.8 eV, predicting that electric and optic properties along the vertical direction could be tuned by an external potential field. Unexpectedly, compared to the lateral device, even if the temperature decreases to 10 K, the on/off ratio of the vertical device maintains a small value, demonstrating a weak regulatory capacity. The variable temperature test indicates that the mixture-structured device performs more like a lateral device, while the electric properties along the vertical direction have little influence on the whole device, indicating that the conductance along the vertical direction is hard to be tuned by temperatures and electrical field. This may provide a new kind of fixed resistor in the integrated circuit devices, promising great potential for next generation electronic and optoelectronic devices.

Conflict of interest

The authors declare that they have no conflict of interest.

Acknowledgments

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Author contribution

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Appendix A. Supplementary material

Supplementary data to this article can be found online at https://doi.org/10.1016/j.scib.2018.11.026.

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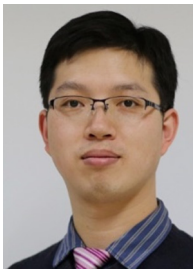

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